DDR2 SDRAM VLP Mini-RDIMM

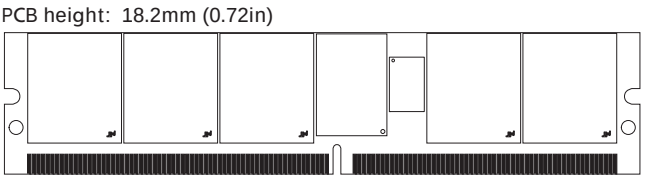
MT18HVS25672(P)K – 2GB
MT18HVS51272(P)K – 4GB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 244-pin, very low profile mini registered dual in-line memory module (VLP Mini-RDIMM)
- Fast data transfer rates: PC2-4200, PC2-5300, or PC2-6400
- 2GB (256 Meg x 8), 4GB (512 Meg x 8)
- Supports ECC error detection and correction
- $V_{DD} = V_{DD}Q = +1.8V$
- $V_{DDSPD} = +1.7V$ to $+3.6V$
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Supports redundant output strobe (RDQS/RDQS#)
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths (BL) 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts
- Dual rank, TwinDie™ (2COB) DRAM devices

Figure 1: 244-Pin VLP Mini-RDIMM



Options	Marking
• Parity	P
• Operating temperature[1]	
– Commercial ($0°C \le T_A \le +70°C$)	None
– Industrial ($–40°C \le T_A \le +85°C$)	I
• Package	
– 244-pin DIMM (Pb-free)	Y
• Frequency/CAS latency[2]	
– 2.5ns @ CL = 5 (DDR2-800)[3]	-80E
– 3.0ns @ CL = 5 (DDR2-667)	-667
– 3.75ns @ CL = 4 (DDR2-533)	-53E

Notes: 1. Contact Micron for industrial temperature module offerings.
2. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.
3. Not available in 4GB module density.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)			^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	800	533	–	12.5	12.5	55
-667	PC2-5300	667	533	400	15	15	55
-53E	PC2-4200	–	533	400	15	15	55

Table 2: Addressing

Parameter	2GB	4GB
Refresh count	8K	8K
Row address	16K (A0–A13)	32K (A0–A14)
Device bank address	8 (BA0, BA1)	8 (BA0–BA2)
Device page size per bank	1KB	1KB
Device configuration	2Gb TwinDie (256 Meg x 8)	4Gb TwinDie (512 Meg x 8)
Column address	1K (A0–A9)	1K (A0–A9)
Module rank address	2 (S0#, S1#)	2 (S0#, S1#)

Table 3: Part Numbers and Timing Parameters – 2GB Modules

Base device: MT47H256M8THN,[1] 2Gb TwinDie DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT18HVS25672(P)KY-80E__	2GB	256 Meg x 8	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT18HVS25672(P)KY-667__	2GB	256 Meg x 8	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT18HVS25672(P)KY-53E__	2GB	256 Meg x 8	4.3 GB/s	3.75ns/533 MT/s	4-4-4

Table 4: Part Numbers and Timing Parameters – 4GB Modules

Base device: MT47H512M8THM,[1] 4Gb TwinDie DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT18HVS51272(P)KY-667__	4GB	512 Meg x 8	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT18HVS51272(P)KY-53E__	4GB	512 Meg x 8	4.3 GB/s	3.75ns/533 MT/s	4-4-4

Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes.
   Example: MT18HVS51272PKY-53EA1.

Pin Assignments and Descriptions

Table 5: Pin Assignments

244-Pin VLP Mini-RDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	32	VSS	63	VDDQ	94	DQS5#
2	VSS	33	DQ24	64	A2	95	DQS5
3	DQ0	34	DQ25	65	VDD	96	VSS
4	DQ1	35	VSS	66	VSS	97	DQ42
5	VSS	36	DQS3#	67	VSS	98	DQ43
6	DQS0#	37	DQS3	68[2]	NF/ PAR_IN	99	VSS
7	DQS0	38	VSS	69	VDD	100	DQ48
8	VSS	39	DQ26	70	A10	101	DQ49
9	DQ2	40	DQ27	71	BA0	102	VSS
10	DQ3	41	VSS	72	VDD	103	SA2
11	VSS	42	CB0	73	WE#	104	NC
12	DQ8	43	CB1	74	VDDQ	105	VSS
13	DQ9	44	VSS	75	CAS#	106	DQS6#
14	VSS	45	DQS8#	76	VDDQ	107	DQS6
15	DQS1#	46	DQS8	77	S1#	108	VSS
16	DQS1	47	VSS	78	ODT1	109	DQ50
17	VSS	48	CB2	79	VDDQ	110	DQ51
18	RESET#	49	CB3	80	NC	111	VSS
19	NC	50	VSS	81	VSS	112	DQ56
20	VSS	51	NC	82	DQ32	113	DQ57
21	DQ10	52	VDDQ	83	DQ33	114	VSS
22	DQ11	53	CKE0	84	VSS	115	DQS7#
23	VSS	54	VDD	85	DQS4#	116	DQS7
24	DQ16	55	BA2	86	DQS4	117	VSS
25	DQ17	56[1]	NF/ ERR_OUT	87	VSS	118	DQ58
26	VSS	57	VDDQ	88	DQ34	119	DQ59
27	DQS2#	58	A11	89	DQ35	120	VSS
28	DQS2	59	A7	90	VSS	121	SA0
29	VSS	60	VDD	91	DQ40	122	SA1
30	DQ18	61	A5	92	DQ41		
31	DQ19	62	A4	93	VSS		

244-Pin VLP Mini-RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
123	VSS	154	DQ28	185	A3	216	NF/ RDQS5#
124	DQ4	155	DQ29	186	A1	217	VSS
125	DQ5	156	VSS	187	VDD	218	DQ46
126	VSS	157	DM3/ RDQS3	188	CK0	219	DQ47
127	DM0/ RDQS0	158	NF/ RDQS3#	189	CK0#	220	VSS
128	NF/ RDQS0#	159	VSS	190	VDD	221	DQ52
129	VSS	160	DQ30	191	A0	222	DQ53
130	DQ6	161	DQ31	192	BA1	223	VSS
131	DQ7	162	VSS	193	VDD	224	NC
132	VSS	163	CB4	194	RAS#	225	NC
133	DQ12	164	CB5	195	VDDQ	226	VSS
134	DQ13	165	VSS	196	S0#	227	DM6/ RDQS6
135	VSS	166	DM8/ RDQS8	197	VDDQ	228	NF/ RDQS6#
136	DM1/ RDQS1	167	NF/ RDQS8#	198	ODT0	229	VSS
137	NF/ RDQS1#	168	VSS	199	A13	230	DQ54
138	VSS	169	CB6	200	VDD	231	DQ55
139	NC	170	CB7	201	NC	232	VSS
140	NC	171	VSS	202	VSS	233	DQ60
141	VSS	172	NC	203	DQ36	234	DQ61
142	DQ14	173	VDDQ	204	DQ37	235	VSS
143	DQ15	174	CKE1	205	VSS	236	DM7/ RDQS7
144	VSS	175	VDD	206	DM4/ RDQS4	237	NF/ RDQS7#
145	DQ20	176[3]	NF/A15	207	NF/ RDQS4#	238	VSS
146	DQ21	177[4]	NF/A14	208	VSS	239	DQ62
147	VSS	178	VDDQ	209	DQ38	240	DQ63
148	DM2/ RDQS2	179	A12	210	DQ39	241	VSS
149	NF/ RDQS2#	180	A9	211	VSS	242	SDA
150	VSS	181	VDD	212	DQ44	243	SCL
151	DQ22	182	A8	213	DQ45	244	VDDSPD
152	DQ23	183	A6	214	VSS		
153	VSS	184	VDDQ	215	DM5/ RDQS5		

Notes:
1. Pin 56 is NF for non-parity and ERR_OUT for parity.
2. Pin 68 is NF for non-parity and PAR_IN for parity.
3. Pin 176 is NF for non-parity and A15 for parity.
4. Pin 177 is NF for 2GB, non-parity and A14 for 2GB, parity; 4GB, non-parity and parity.

Figure 2: Pin Descriptions

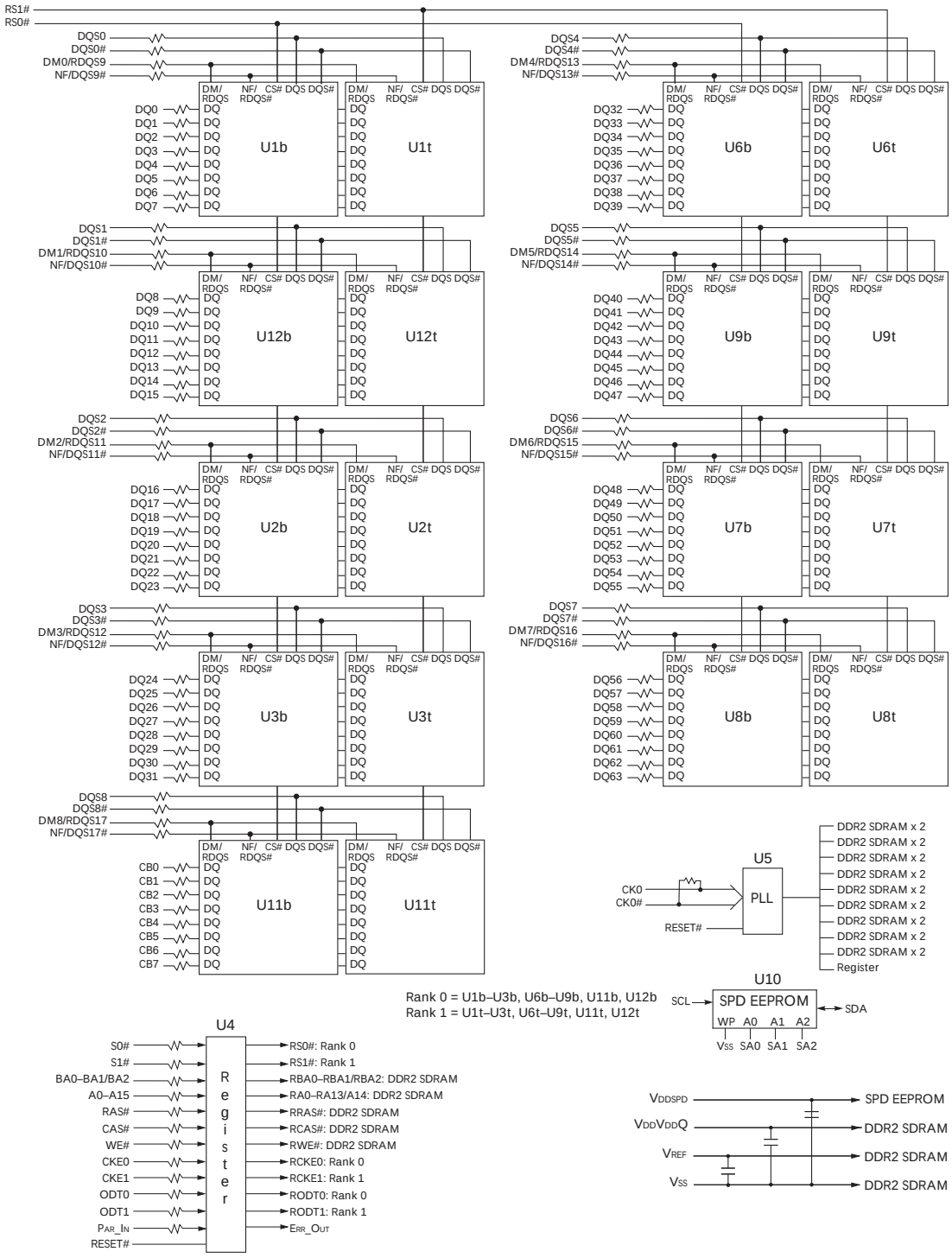
Symbol	Type	Description
A0–A15	Input (SSTL_18)	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA1/BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LM command. A0–A13 (2GB) and A0–A14 (4GB). A0–A15 are connected for parity.
BA0–BA2	Input (SSTL_18)	**Bank address inputs:** BA0–BA1/BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1/BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.
CK0, CK0#	Input (SSTL_18)	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0, CKE1#	Input (SSTL_18)	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
ODT0, ODT1	Input (SSTL_18)	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled ODT is only applied to each of the following pins: DQ, DQS, DQS#, RDQS, RDQS#, CB, and DM. The ODT input will be ignored if disabled via the LOAD MODE (LM) command.
PAR_IN	Input (SSTL_18)	Parity bit for the address and control bus. The non-parity version is not used.
RAS#, CAS#, WE#	Input (SSTL_18)	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.
S0#, S1#	Input (SSTL_18)	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# provides for external rank selection on systems with multiple ranks. S# is considered part of the command code.
SA0–SA2	Input (SSTL_18)	**Presence-detect address inputs:** These pins are used to configure the presence-detect device.
SCL	Input (SSTL_18)	**Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module.
CB0–CB7	I/O (SSTL_18)	**Check bits.**
DM0–DM8 (RDQS0–RDQS8)	I/O (SSTL_18)	**Data input mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. If RDQS is enabled, RDQS0#–RDQS8# are used only during the READ command. If RDQS is disabled, RDQS0–RDQS8 become DM0–DM8 and RDQS0#–RDQS8 are not used.
DQ0–DQ63	I/O (SSTL_18)	**Data input/output:** Bidirectional data bus.
DQS0–DQS8, DQS0#–DQS8#	I/O (SSTL_18)	**Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LM command.
SDA	I/O (SSTL_18)	**Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
ERR_OUT	Output (open drain)	Parity error found on the address and control bus. The non-parity version is not used.

Figure 2: Pin Descriptions (continued)

Symbol	Type	Description
V_{DD}/V_{DD}Q	Supply	**Power supply:** 1.8V ±0.1V.
V_{DDSPD}	Supply	**Serial EEPROM positive power supply:** +1.7V to +3.6V.
V_{REF}	Supply	SSTL_18 reference voltage (V_{DD}/2).
V_{SS}	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.
NF	–	**No function:** Connected within the module but provides no functionality.

Functional Block Diagram

Figure 3: Functional Block Diagram



General Description

The MT18HVS25672(P)K and MT18HVS51272(P)K DDR2 SDRAM modules are high-speed, CMOS, dynamic random access 2GB and 4GB memory modules organized in a x72 configuration. DDR2 SDRAM modules use internally configured (2Gb TwinDie or 4Gb TwinDie), 8-bank DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

PLL and Register Operation

DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The register(s) and PLL reduce address, command, control, and clock signal loading by isolating DRAM from the system controller. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

Parity Option

If provided from the system memory controller, (PAR_IN) is compared within the register to the command and address inputs of the register. An even number of ones among these inputs is defined as valid parity. In the case that invalid parity is detected, ERR_OUT will be set LOW.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to VSS on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 6 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in the device data sheet are not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 6: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
V_{DD}/V_{DDQ}	V_{DD}/V_{DDQ} supply voltage relative to V_{SS}		–0.5	+2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		–0.5	+2.3	V
I_I	Input leakage current; Any input $0V \le V_{IN} \le V_{DD}$; V_{REF} input $0V \le V_{IN} \le 0.95V$ (All other pins not under test = 0V)	Address inputs RAS#, CAS#, WE#, S#, CKE, ODT, BA	–5	+5	µA
		CK, CK#	–250	+250	
		DM	–10	+10	
I_{OZ}	Output leakage current; $0V \le V_{OUT} \le V_{DDQ}$; DQs and ODT are disabled	DQ, DQS, DQS#	–10	+10	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = valid V_{REF} level		–36	+36	µA
T_A	Module ambient operating temperature	Commercial	0	+70	°C
		Industrial	–40	+85	°C
T_C[1]	DDR2 SDRAM component case operating temperature[2]	Commercial	0	+85	°C
		Industrial	–40	+95	°C

Notes:
1. Refresh rate is required to double when $85°C < T_C \le 95°C$.
2. For further information, refer to technical note TN-00-08, "Thermal Applications," available on Micron's Web site.

Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations. JEDEC modules are currently designed using simulations to close timing budgets.

Component AC Timing and Operating Specifications

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 7.

Table 7: Module and Component Speed Grades

Module Speed Grade	Component Speed Grade
-80E	-25E
-667	-3
-53E	-37E

IDD Specifications

Table 8: IDD Specifications and Conditions – 2GB

Values are shown for the MT47H256M8THN DDR2 SDRAM only and are computed from values specified in the 2Gb TwinDie (256 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E	-667	-53E	Units
Operating one bank active-precharge current: ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0	918	873	738	mA
Operating one bank active-read-precharge current: IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1	1,098	1,008	963	mA
Precharge power-down current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P	126	126	126	mA
Precharge quiet standby current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q	513	423	423	mA
Precharge standby current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N	558	468	468	mA
Active power-down current: All device banks open; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3P	333	333	333	mA
	Slow PDN exit MR[12] = 1		153	153	153	mA
Active standby current: All device banks open; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N	648	603	513	mA
Operating burst write current: All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W	1,548	1,323	1,233	mA
Operating burst read current: All device banks open, continuous burst reads; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R	1,548	1,323	1,233	mA
Burst refresh current: ^{t}CK = ^{t}CK (IDD); REFRESH command at every ^{t}RFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5	2,223	2,043	1,998	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6	126	126	126	mA
Operating bank interleave read current: All device banks interleaving reads; IOUT= 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD) - 1 × ^{t}CK (IDD); ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RRD = ^{t}RRD (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching		IDD7	3,123	2,628	2,538	mA

Table 9: IDD Specifications and Conditions – 4GB

Values are shown for the MT47H512M8THM DDR2 SDRAM only and are computed from values specified in the 4Gb TwinDie (512 Meg x 8) component data sheet

Parameter/Condition		Symbol	-667	-53E	Units
Operating one bank active-precharge current: tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0	1,017	927	mA
Operating one bank active-read-precharge current: IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1	1,422	1,062	mA
Precharge power-down current: All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are floating		IDD2P	144	144	mA
Precharge quiet standby current: All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q	567	477	mA
Precharge standby current: All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N	657	567	mA
Active power-down current: All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3P	432	387	mA
	Slow PDN exit MR[12] = 1		162	162	mA
Active standby current: All device banks open; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N	612	522	mA
Operating burst write current: All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W	1,467	1,287	mA
Operating burst read current: All device banks open, Continuous burst reads; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R	1,647	1,467	mA
Burst refresh current: tCK = tCK (IDD); REFRESH command at every tRFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5	2,637	2,457	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6	144	144	mA
Operating bank interleave read current: All device banks interleaving reads; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD) - 1 × tCK (IDD); tCK = tCK (IDD), tRC = tRC (IDD), tRRD = tRRD (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching		IDD7	3,177	2,772	mA

Register and PLL Specifications

Table 10: Register Specifications
SSTU32865 device or equivalent JESD82-19

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	$V_{IH(DC)}$	Address, control, command	SSTL_18	$V_{REF(DC)}$ + 125	V_{DDQ} + 250	mV
DC low-level input voltage	$V_{IL(DC)}$	Address, control, command	SSTL_18	0	$V_{REF(DC)}$ - 125	mV
AC high-level input voltage	$V_{IH(AC)}$	Address, control, command	SSTL_18	$V_{REF(DC)}$ + 250	V_{DD}	mV
AC low-level input voltage	$V_{IL(AC)}$	Address, control, command	SSTL_18	0	$V_{REF(DC)}$ - 250	mV
Output high voltage	V_{OH}	Parity output	LVCMOS	1.2	–	V
Output low voltage	V_{OL}	Parity output	LVCMOS	–	0.5	V
Input current	I_I	All pins	V_I = V_{DDQ} or V_{SSQ}	–5	5	µA
Static standby	I_{DD}	All pins	RESET# = V_{SSQ} (I_O = 0)	–	200	µA
Static operating	I_{DD}	All pins	RESET# = V_{SSQ}; V_I = $V_{IH(AC)}$ or $V_{IL(DC)}$ I_O = 0	–	80	mA
Dynamic operating – clock tree	I_{DDD}	n/a	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I_O = 0; CK and CK# switching 50% duty cycle	–	Varies by manufacturer	µA
Dynamic operating (per each input)	I_{DDD}	n/a	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I_O = 0; CK and CK# switching 50% duty cycle; One data input switching at $^tCK/2$, 50% duty cycle	–	Varies by manufacturer	µA
Input capacitance (per device, per pin)	C_I	All inputs except RESET#	V_I = V_{REF} ±250mV; V_{DDQ} = 1.8V	2.5	3.5	pF
Input capacitance (per device, per pin)	C_I	RESET#	V_I = V_{DDQ} or V_{SSQ}	–	Varies by manufacturer	pF

Notes: 1. Timing and switching specifications for the register listed above are critical for proper operation of the DDR2 SDRAM registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC-standard JESD82.

Table 11: PLL Specifications
CU877 device or equivalent JESD82-8.01

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	V_{IH}	RESET#	LVCMOS	0.65 × V_{DD}	–	V
DC low-level input voltage	V_{IL}	RESET#	LVCMOS	–	0.35 × V_{DD}	V
Input voltage (limits)	V_{IN}	RESET#, CK, CK#	–	–0.3	V_{DDQ} + 0.3	V
DC high-level input voltage	V_{IH}	CK, CK#	Differential input	0.65 × V_{DD}	–	V
DC low-level input voltage	V_{IL}	CK, CK#	Differential input	–	0.35 × V_{DD}	V
Input differential-pair cross voltage	V_{IX}	CK, CK#	Differential input	(V_{DDQ}/2) - 0.15	(V_{DDQ}/2) + 0.15	V
Input differential voltage	$V_{ID(DC)}$	CK, CK#	Differential input	0.3	V_{DDQ} + 0.4	V
Input differential voltage	$V_{ID(AC)}$	CK, CK#	Differential input	0.6	V_{DDQ} + 0.4	V
Input current	I_I	RESET#	V_I = V_{DDQ} or V_{SSQ}	–10	+10	µA
		CK, CK#	V_I = V_{DDQ} or V_{SSQ}	–250	+250	µA
Output disabled current	I_{ODL}	–	RESET# = V_{SSQ}; V_I = $V_{IH(AC)}$ or $V_{IL(DC)}$	100	–	µA
Static supply current	I_{DDLD}	–	CK = CK# = LOW	–	500	µA
Dynamic supply	I_{DD}	n/a	CK, CK# = 410 MHz, all outputs open (not connected to PCB)	–	300	mA
Input capacitance	C_{IN}	Each input	V_I = V_{DDQ} or V_{SSQ}	2	3	pF

Table 12: PLL Clock Driver Timing Requirements and Switching Characteristics

Parameter	Symbol	Min	Max	Units
Stabilization time	^tL	–	15	µs
Input clock slew rate	$^tslr(i)$	1.0	4	V/ns
SSC modulation frequency	–	30	33	kHz
SSC clock input frequency deviation	–	0	–0.50	%
PLL loop bandwidth (–3dB from unity gain)	–	2.0	–	MHz

Notes: 1. PLL timing and switching specifications are critical for proper operation of the DDR2 DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC-standard JESD82.

Serial Presence-Detect

Table 13: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DDSPD}	I_{LI}	0.10	3.0	µA
Output leakage current: V_{OUT} = GND to V_{DDSPD}	I_{LO}	0.05	3.0	µA
Standby current	I_{SB}	1.6	4.0	µA
Power supply current, READ: SCL clock frequency = 100 kHz	I_{CC_R}	0.4	1.0	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	I_{CC_W}	2.0	3.0	mA

Table 14: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3	–	µs	
Data-out hold time	^tDH	200	–	ns	
SDA and SCL fall time	^tF	–	300	ns	2
Data-in hold time	$^tHD:DAT$	0	–	µs	
Start condition hold time	$^tHD:STA$	0.6	–	µs	
Clock HIGH period	^tHIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^tI	–	50	ns	
Clock LOW period	^tLOW	1.3	–	µs	
SDA and SCL rise time	^tR	–	0.3	µs	2
SCL clock frequency	^fSCL	–	400	kHz	
Data-in setup time	$^tSU:DAT$	100	–	ns	
Start condition setup time	$^tSU:STA$	0.6	–	µs	3
Stop condition setup time	$^tSU:STO$	0.6	–	µs	
WRITE cycle time	^tWRC	–	10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Table 15: Serial Presence-Detect Matrix

Byte	Description	Entry (Version)	2GB	4GB[1]
0	Number of SPD bytes used by Micron	128	80	80
1	Total number of bytes in SPD device	256	08	08
2	Fundamental memory type	DDR2 SDRAM	08	08
3	Number of row addresses on assembly	14 or 15	0E	0F
4	Number of column addresses on assembly	10	0A	0A
5	DIMM height and module ranks	18.2mm, dual rank	11	11
6	Module data width	72	48	48
7	Reserved	0	00	00
8	Module voltage interface levels	SSTL 1.8V	05	05
9	SDRAM cycle time, ^{t}CK (CL = MAX value, see byte 18)	-80E -667 -53E	25 30 3D	– 30 3D
10	SDRAM access from clock,^{t}AC (CL = MAX value, see byte 18)	-80E -667 -53E	40 45 50	– 45 50
11	Module configuration type	ECC ECC and parity	02 06	02 06
12	Refresh rate/type	7.81µs/SELF	82	82
13	SDRAM device width (primary SDRAM)	8	08	08
14	Error-checking SDRAM data width	8	08	08
15	Reserved	0	00	00
16	Burst lengths supported	4, 8	0C	0C
17	Number of banks on SDRAM device	8	08	08
18	CAS latencies supported	-80E (5, 4) -667 (5, 4, 3) -53E (4, 3)	30 38 18	– 38 18
19	Module thickness	–	01	01
20	DDR2 DIMM type	Registered VLP Mini-RDIMM	10	10
21	SDRAM module attributes	1 PLL, 1 Reg	04	04
22	SDRAM device attributes: weak driver (01) and 50Ω ODT (03)	-80E/-667 -53E	03 01	–/03 01
23	SDRAM cycle time, ^{t}CK, MAX CL - 1	80E/-667 -53E	3D 50	–/3D 50
24	SDRAM access from CK, ^{t}AC, MAX CL - 1	-80E -667 -53E	40 45 50	– 45 50
25	SDRAM cycle time, ^{t}CK, MAX CL - 2	-80E -667 -53E	00 50 00	– 50 00
26	SDRAM access from CK, ^{t}AC, MAX CL - 2	-80E -667 -53E	00 45 00	– 45 00
27	MIN row precharge time, ^{t}RP	-80E -667/-53E	32 3C	– 3C
28	MIN row active-to-row active, ^{t}RRD	–	1E	1E
29	MIN RAS#-to-CAS# delay, ^{t}RCD	-80E -667/-53E	32 3C	– 3C
30	MIN active-to-precharge time, ^{t}RAS	–	2D	2D

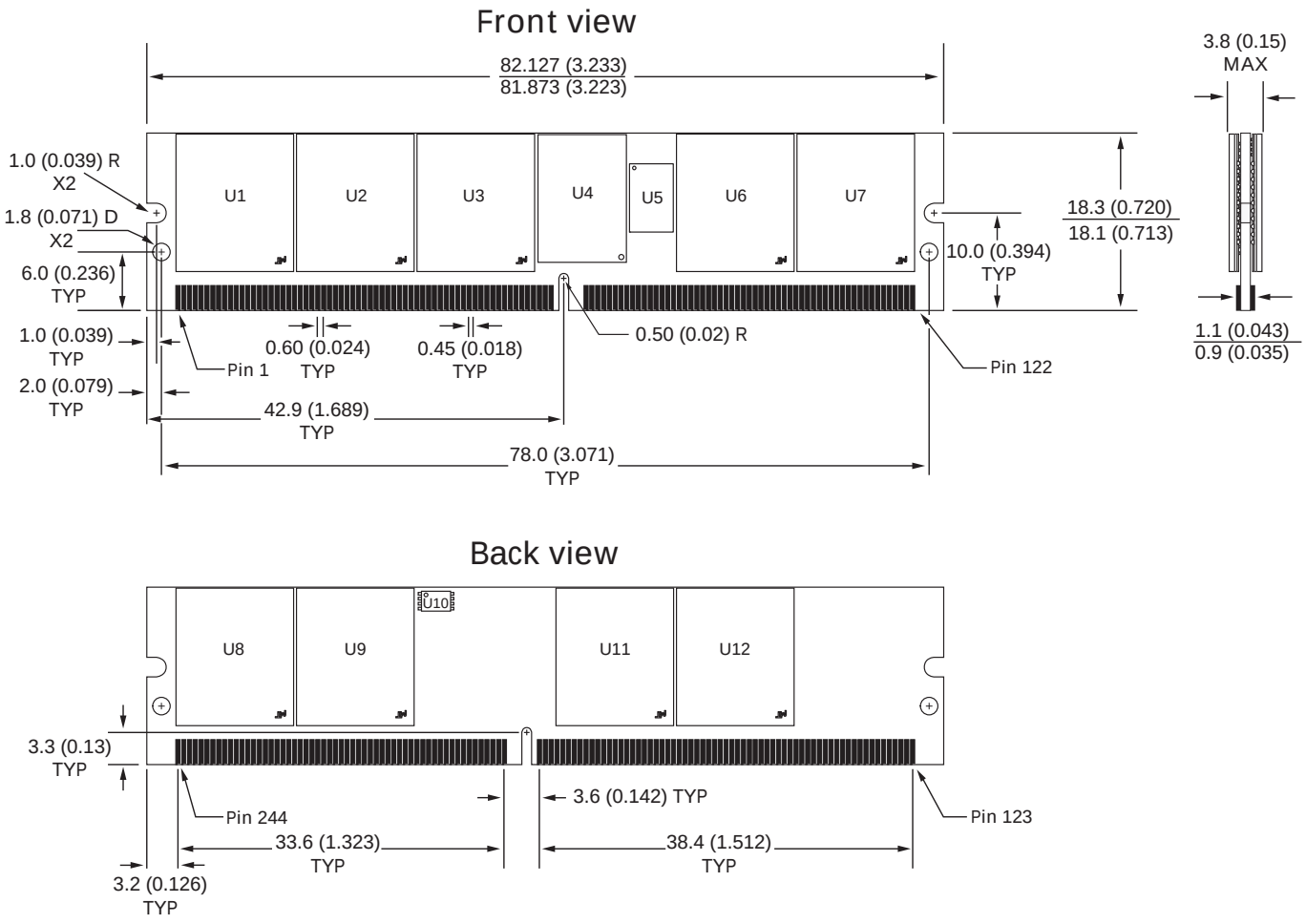
Table 15: Serial Presence-Detect Matrix (continued)

Byte	Description	Entry (Version)	2GB	4GB[1]
31	Module rank density	1GB, 2GB	01	02
32	Address and command setup time, $^{t}IS_{b}$	-80E -667 -53E	17 20 25	– 20 25
33	Address and command hold time, $^{t}IH_{b}$	-80E -667 -53E	25 27 37	– 27 37
34	Data/data mask input setup time, $^{t}DS_{b}$	-80E -667/-53E	05 10	– 10
35	Data/data mask input hold time, $^{t}DH_{b}$	-80E -667 -53E	12 17 22	– 17 22
36	Write recovery time, ^{t}WR	–	3C	3C
37	WRITE-to-READ command delay, ^{t}WTR	–	1E	1E
38	READ-to-PRECHARGE command delay, ^{t}RTP	–	1E	1E
39	Memory analysis probe	–	00	00
40	Extension for bytes 41 and 42	-80E -667/-53E	36 06	– 06
41	MIN active-to-active/refresh time, ^{t}RC[2]	-80E -667/-53E	39 3C	– 3C
42	MIN AUTO REFRESH to ACTIVE/AUTO REFRESH command period, ^{t}RFC	–	7F	C5
43	SDRAM device MAX cycle time, ^{t}CK (MAX)	–	80	80
44	SDRAM device MAX DQS–DQ skew time, $^{t}DQSQ$	-80E -667 -53E	14 18 1E	– 18 1E
45	SDRAM device MAX read data hold skew factor, ^{t}QHS	-80E -667 -53E	1E 22 28	– 22 28
46	PLL relock time	–	0F	0F
47–61	Optional features, not supported	–	00	00
62	SPD revision	Release 1.2	12	12
63	Checksum for bytes 0–62 ECC/ECC and parity	-80E -667 -53E	14/18 D0/D4 7B/7F	– 18/1C C3/C7
64	Manufacturer's JEDEC ID code	Micron	2C	2C
65–71	Manufacturer's JEDEC ID code	(continued)	00	00
72	Manufacturing location	1–12	Variable data	Variable data
73–90	Module part number (ASCII)	–	Variable data	Variable data
91	PCB identification code	1–9	01–09	01–09
92	PCB identification code (continued)	–	00	00
93	Year of manufacture in BCD	–	Variable data	Variable data
94	Week of manufacture in BCD	–	Variable data	Variable data
95–98	Module serial number	–	Variable data	Variable data
99–127	Reserved for manufacturer-specific data	–	00	00
128–255	Reserved for customer-specific data	–	FF	FF

Notes:
1. The 4GB module is not available in the -80E speed grade.
2. The ^{t}RC SPD values shown are JEDEC DDR2 device specification values. The actual Micron DDR2 device specification is ^{t}RC = 55ns for all speed grades.

Module Dimensions

Figure 4: 244-Pin DDR2 VLP Mini-RDIMM



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

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