MOSFETs Silicon N-Channel MOS (U-MOSⅤ)

TPCL4202

1. Applications

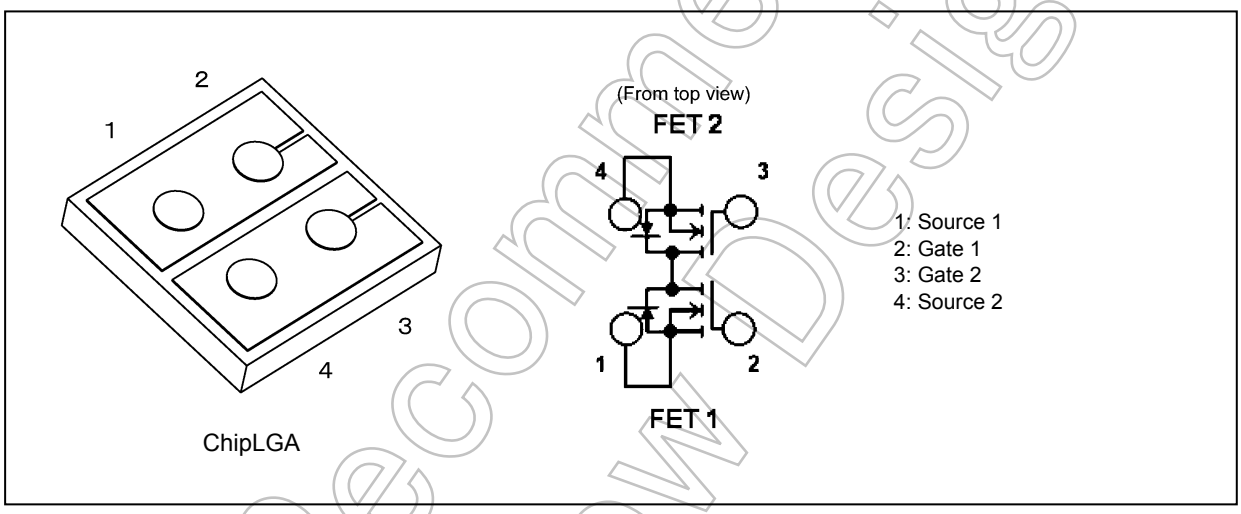
- Dedicated to Single-Cell Lithium-Ion Secondary Battery Applications

Note: The product(s) described herein should not be used for any other application.

2. Features

(1) Small, thin package
(2) Low source-source on-resistance: $R_{SS(ON)}$ = 28 mΩ (typ.) (V_{GS} = 4.5 V)
(3) Low leakage current: I_{SSS} = 10 μA (max) (V_{SS} = 30 V)
(4) Enhancement mode: V_{th} = 0.5 to 1.2 V (V_{SS} = 10 V, I_S = 200 μA)
(5) Common drain

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) (T_a = 25°C unless otherwise specified)

Characteristics			Symbol	Rating	Unit
Source-source voltage			V_{SSS}	30	V
Gate-source voltage			V_{GSS}	±12	
Source current (DC)		(Note 1)	I_S	6	A
Source current (pulsed)		(Note 1)	I_{SP}	24	
Power dissipation	(t = 10 s)	(Note 2), (Note 4)	P_D	0.50	W
Power dissipation	(t = 10 s)	(Note 3), (Note 4)	P_D	1.65	W
Channel temperature			T_{ch}	150	°C
Storage temperature			T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

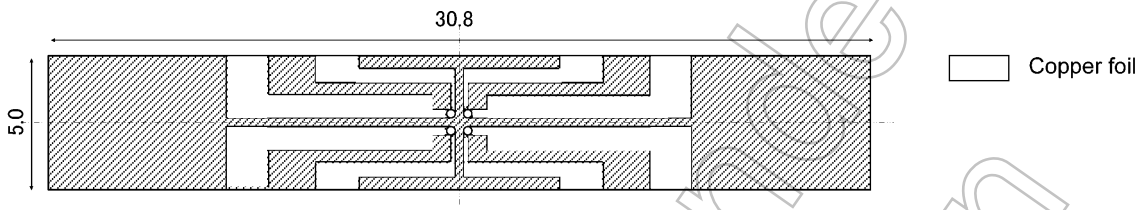
Not Recommended for New Design

Start of commercial production
2009-04

5. Thermal Characteristics

Characteristics			Symbol	Max	Unit
Channel-to-ambient thermal resistance	(t = 10 s)	(Note 2), (Note 4)	$R_{th(ch-a)}$	250	°C/W
Channel-to-ambient thermal resistance	(t = 10 s)	(Note 3), (Note 4)	$R_{th(ch-a)}$	75.8	°C/W

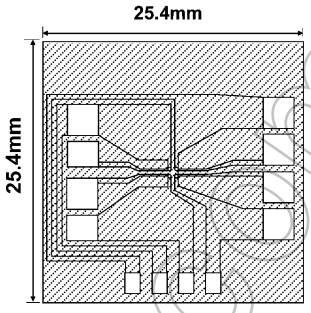
Note 1: Ensure that the channel temperature does not exceed 150°C.
Note 2: Device mounted on a glass-epoxy board (a), Figure 5.1
Note 3: Device mounted on a glass-epoxy board (b), Figure 5.2
Note 4: Equal voltage applied to FET1 and FET2.



30.8 × 5.0 × 0.6（Unit: mm）

FR-4　Glass-epoxy board（One-layer）

Fig. 5.1　Device Mounted on a Glass-Epoxy Board (a)



25.4 × 25.4 × 0.6（Unit: mm）

FR-4　Glass-epoxy board（four-layer）

Copper foil

Fig. 5.2　Device Mounted on a Glass-Epoxy Board (b)

Note:　This transistor is sensitive to electrostatic discharge and should be handled with care.

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6. Safety Precautions

This section lists important precautions which users of semiconductor devices (and anyone else) should observe in order to avoid injury to human body and damage to property, and to ensure safe and correct use of our products. Please be sure that you understand the meanings of the labels and graphic symbols described below before you move on to the detailed descriptions of the precautions, and comply with the precautions stated.

Explanation of Labels

⚠WARNING
Indicates a hazardous situation which, if not avoided, could result in death or serious injury[1].

Explanation of Graphic Symbols

Instructions
Indicates actions that must be undertaken for safety purposes.

1: Serious injury includes blindness, wounds, burns (low and high temperature), electric shock, fractures, and poisoning, etc. with long-lasting effects or that require hospitalization and/or long-term hospital visits for treatment.

⚠WARNING	
Instructions	【Handling Precaution for Power MOSFET in use of Protection Circuit for Battery Pack】 Use a unit, for example PTC Thermistor, which can shut off the power supply if a short-circuit occurs. If the power supply is not shut off on the occurring short-circuit, a large short-circuit current will flow continuously, which may cause the device to catch fire or smoke. The product listed in this document is intended for usage in Lithium Ion Battery charge and discharge control application. So it is responsible for customer when using the product in the different application.

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7. Electrical Characteristics

7.1. Static Characteristics (T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	(Note 5)	I_{GSS}	V_{GS} = ±12 V, V_{SS} = 0 V	—	—	±0.1	μA
Source cut-off current	(Note 5)	I_{SSS}	V_{SS} = 30 V, V_{GS} = 0 V	—	—	10	
Source-source breakdown voltage	(Note 5)	$V_{(BR)SSS}$	I_S = 10 mA, V_{GS} = 0 V	30	—	—	V
		$V_{(BR)SSX}$	I_S = 10 mA, V_{GS} = -12 V	18	—	—	
Gate threshold voltage	(Note 5)	V_{th}	V_{SS} = 10 V, I_S = 200 μA	0.5	—	1.2	
Source-source on-resistance	(Note 6)	$R_{SS(ON)}$	V_{GS} = 2.5 V, I_S = 3 A	31	46	64	mΩ
			V_{GS} = 3.1 V, I_S = 3 A	28	40	50	
			V_{GS} = 4.0 V, I_S = 3 A	25	30	42	
			V_{GS} = 4.5 V, I_S = 3 A	24	28	40	

7.2. Dynamic Characteristics (T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	(Note 5)	C_{iss}	V_{SS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	780	—	pF
Reverse transfer capacitance	(Note 5)	C_{rss}		—	70	—	
Output capacitance	(Note 5)	C_{oss}		—	130	—	
Switching time (rise time)	(Note 5)	t_r	See Figure 7.2.1.	—	70	—	ns
Switching time (turn-on time)	(Note 5)	t_{on}		—	105	—	
Switching time (fall time)	(Note 5)	t_f		—	125	—	
Switching time (turn-off time)	(Note 5)	t_{off}		—	310	—	

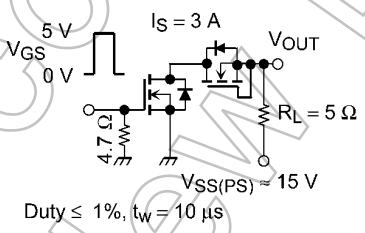

Fig. 7.2.1 Switching Time Test Circuit

7.3. Gate Charge Characteristics (T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	(Note 5)	Q_g	$V_{SS(PS)}$ ≈ 24 V, V_{GS} = 5 V, I_S = 6 A	—	10	—	nC
Gate-source charge 1	(Note 5)	Q_{gs1}		—	2	—	

7.4. Source-Source Characteristics (T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage	(Note 7)	V_{SSF}	I_{SR} = 3 A, V_{GS} = 0 V	—	—	-1.2	V

Note 5: FET1 is measured with the gate and source pins of FET2 shorted. FET2 is measured with the gate and source pins of FET1 shorted.

Note 6: Measured with the indicated gate-to-source voltage (V_{GS}) applied to both FET1 and FET2.

Note 7: FET1 is measured with 4.5 V applied between the gate and source pins of FET2. FET2 is measured with 4.5 V applied between the gate and source pins of FET1.

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8. Marking

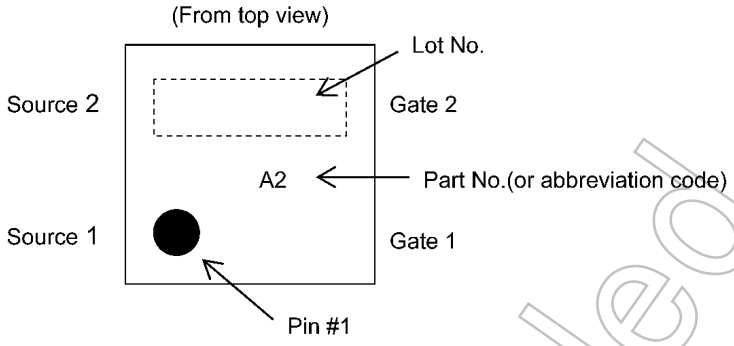

Fig. 8.1 Marking

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9. Mounting Condition

This device should be soldered onto a pc board with up to two reflow passes at the recommended reflow conditions. The second reflow process should be performed within two weeks after the first reflow process.

9.1. Using Infrared Reflow

(1) It is recommended the top and bottom heating method with long or medium infrared rays. (See Figure 9.1.1.)

(2) Figure 9.1.2 shows the recommended temperature profile for using eutectic solder. Figure 9.1.3 shows the recommended temperature profile for using lead (Pb)-free solder. Complete the infrared ray reflow process with a maximum package surface temperature of 260℃, within 30 to 50 seconds when a package surface temperature is 230℃ or higher (See Figure 9.1.3).

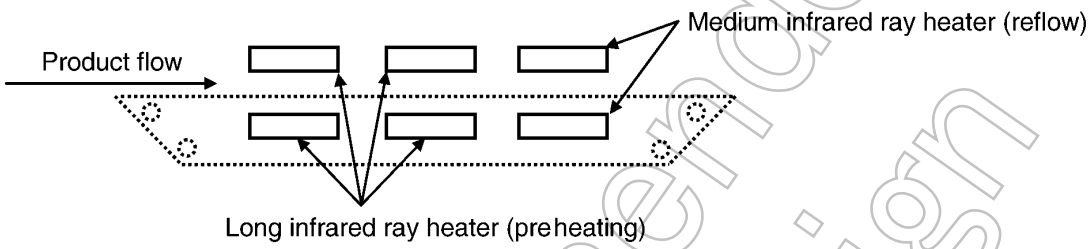

Fig. 9.1.1 Heating the Top and Bottom with Long or Medium Infrared Rays

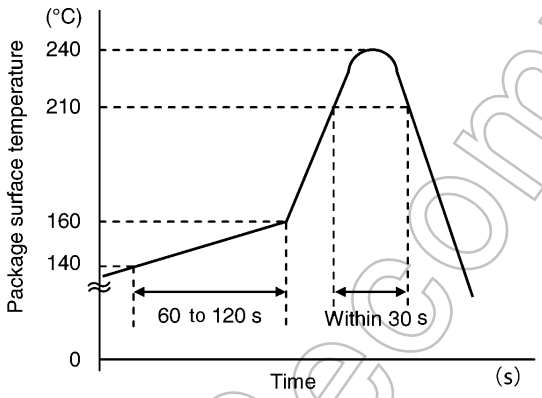

Fig. 9.1.2 Eutectic Recommended Temperature Profile

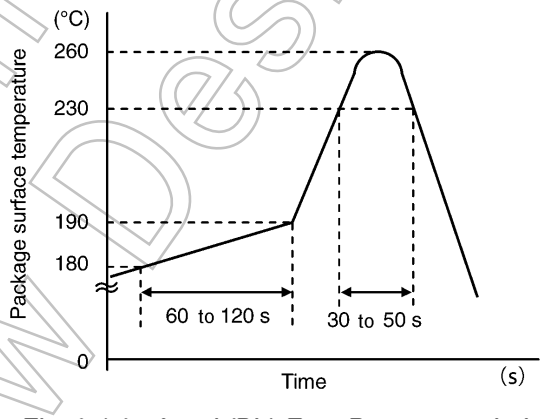

Fig. 9.1.3 Lead (Pb)-Free Recommended Temperature Profile

9.2. Using Hot Air Reflow

For an example of a recommended temperature profile, refer to Figures 9.1.2 and 9.1.3.

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9.3. Mechanical Stress

This device is very small and thin. Excessive mechanical stress may damage the package and/or chip. To avoid damage to the device, the distortion factor should be kept below 2000 με or within the shaded area in Figure 9.3.1. Keep in mind that the stress applied to the device varies, depending on the shape, material, trace patterns, parts layout and other conditions of the pc board. Thus the integrity of the device should be tested on the actual application board. In addition, the end product should provide adequate headroom above the top (marking) side of the device so that no mechanical stress will be applied to it.

The distortion factor (ε) is given by:

ε = 6 h S/ (L × L), h: Board thickness, S = Bend, L = Support-to-support distance

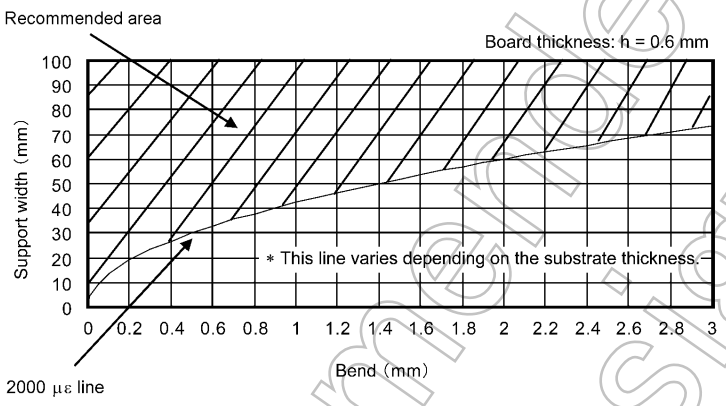

Fig. 9.3.1 Support-to-Support Distance vs. Bending

9.4. Test Method

Test method (reference standard JEITA ED-4702A):

The test board is placed on supports with the device face-down. The supports are placed with a distance of 24 mm as shown in Figure 9.4.1 below. Stress is applied to the test board as shown in Figure 9.4.2.

Test board: FR-4 glass epoxy board measuring 30.8 mm × 5 mm × 0.6 mm

A rigid pc board with a thickness of 0.4 mm or more should be used for actual applications.

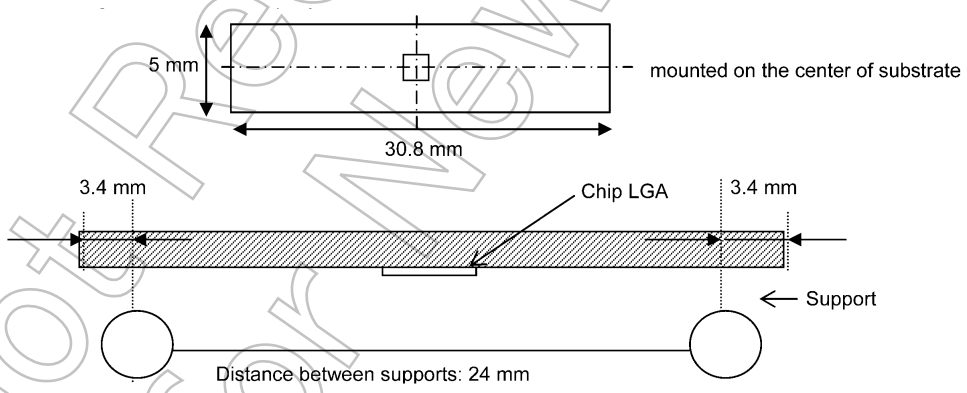

Fig. 9.4.1 Placement

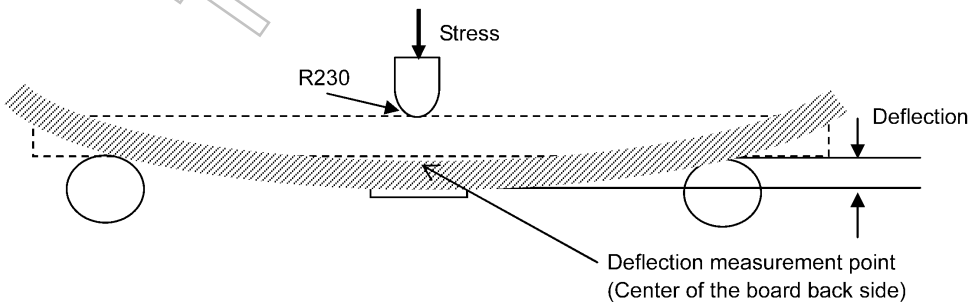

Fig. 9.4.2 During Testing

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10. Characteristics Curves (Note)

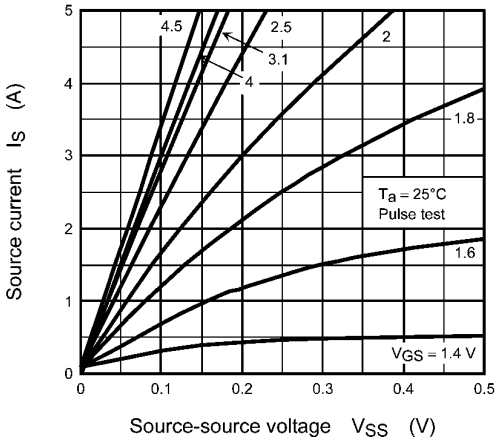

Fig. 10.1 I_S - V_{SS} (Note 6)

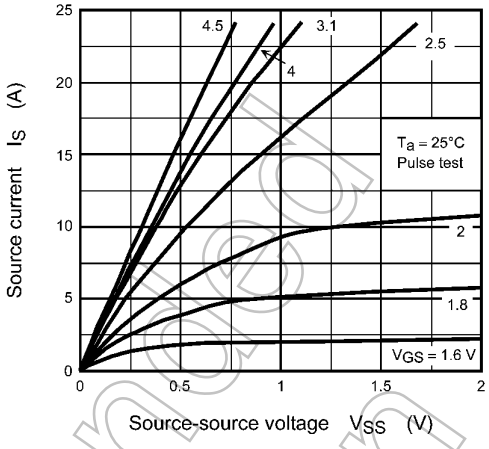

Fig. 10.2 I_S - V_{SS} (Note 6)

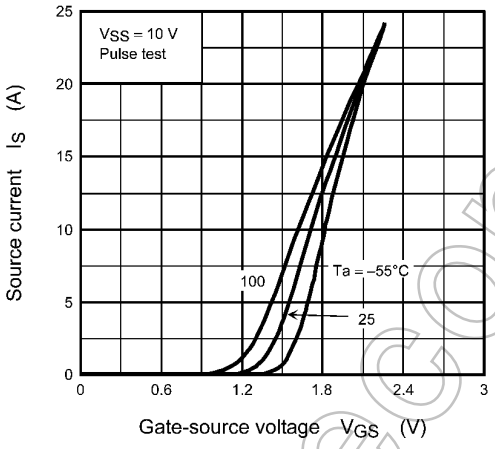

Fig. 10.3 I_S - V_{GS} (Note 5)

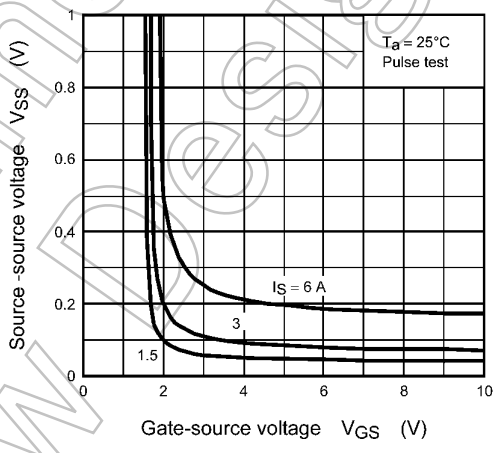

Fig. 10.4 V_{SS} - V_{GS} (Note 6)

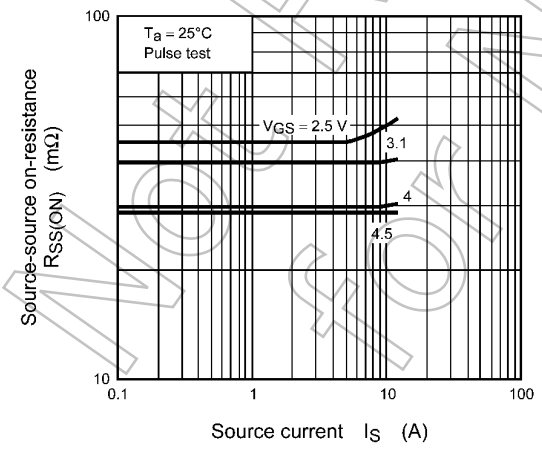

Fig. 10.5 $R_{SS(ON)}$ - I_S (Note 6)

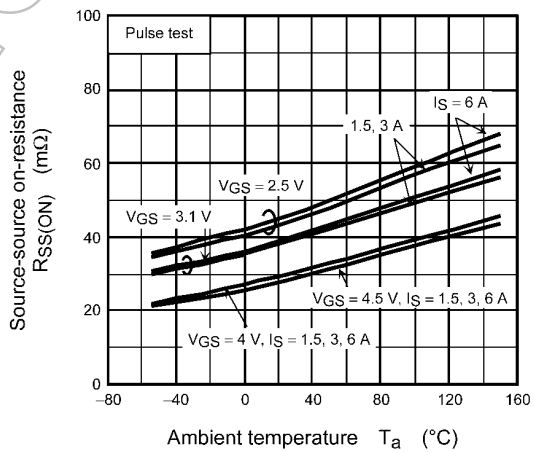

Fig. 10.6 $R_{SS(ON)}$ - T_a (Note 6)

Not Recommended for New Design

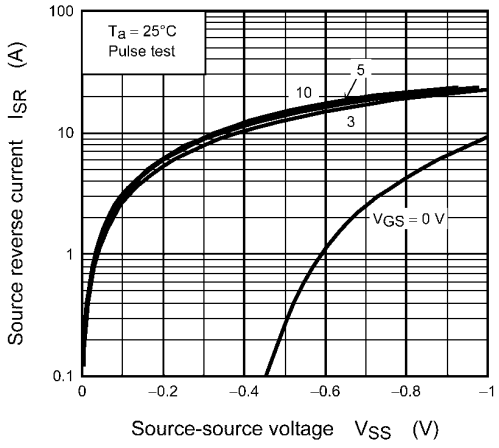

Fig. 10.7 I_{SR} - V_{SS} (Note 7)

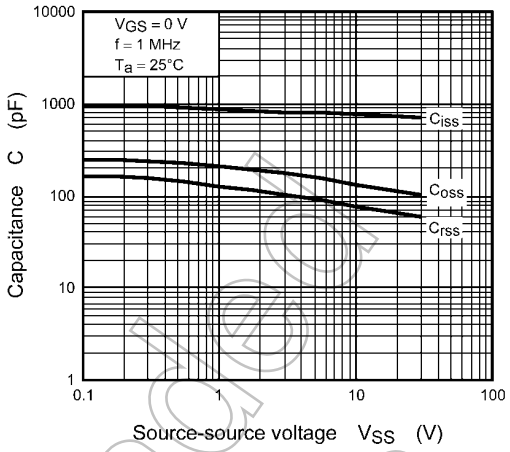

Fig. 10.8 Capacitance - V_{SS} (Note 5)

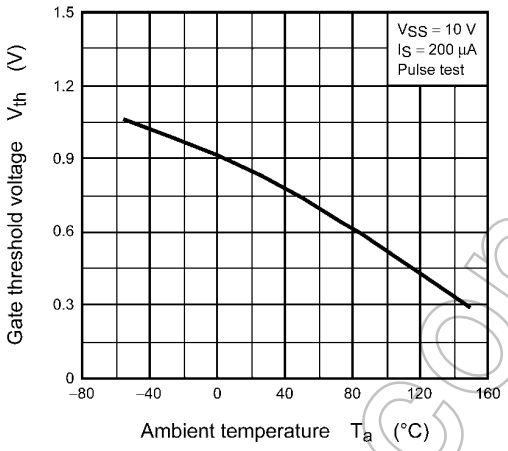

Fig. 10.9 V_{th} - T_a (Note 5)

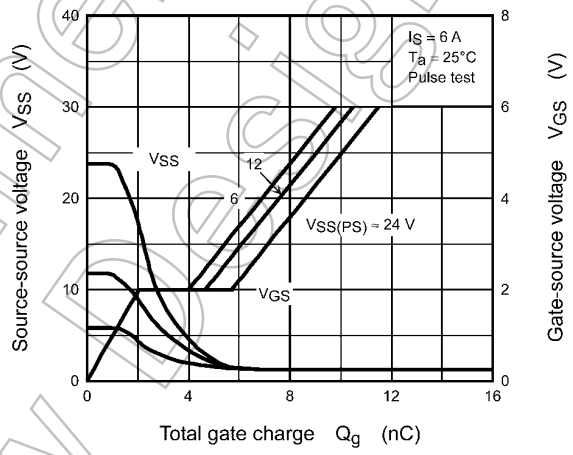

Fig. 10.10 Dynamic Input/Output Characteristics (Note 5)

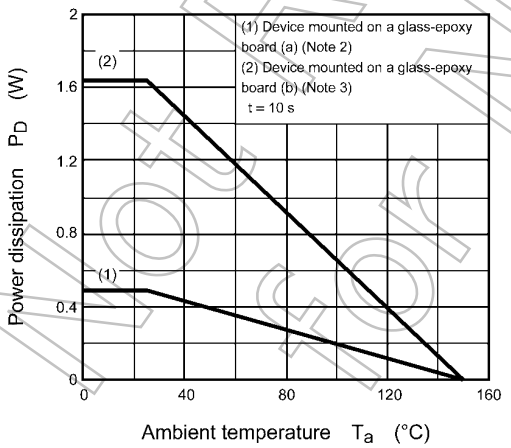

Fig. 10.11 P_D - T_a (Note 4) (Guaranteed Maximum)

Not Recommended for New Design

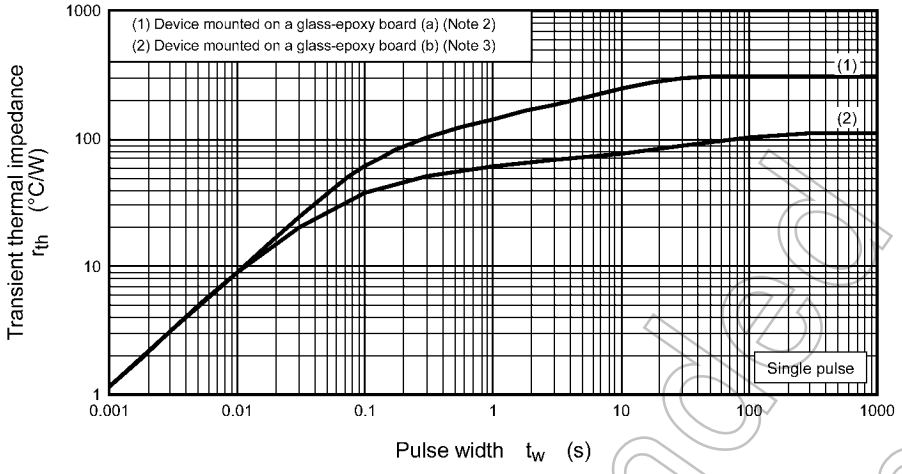

Fig. 10.12 r_{th} - t_w (Note 4) (Guaranteed Maximum)

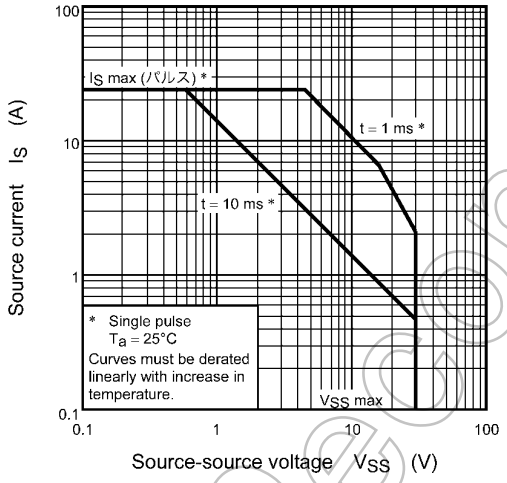

Fig. 10.13 Safe Operating Area (Note 4) (Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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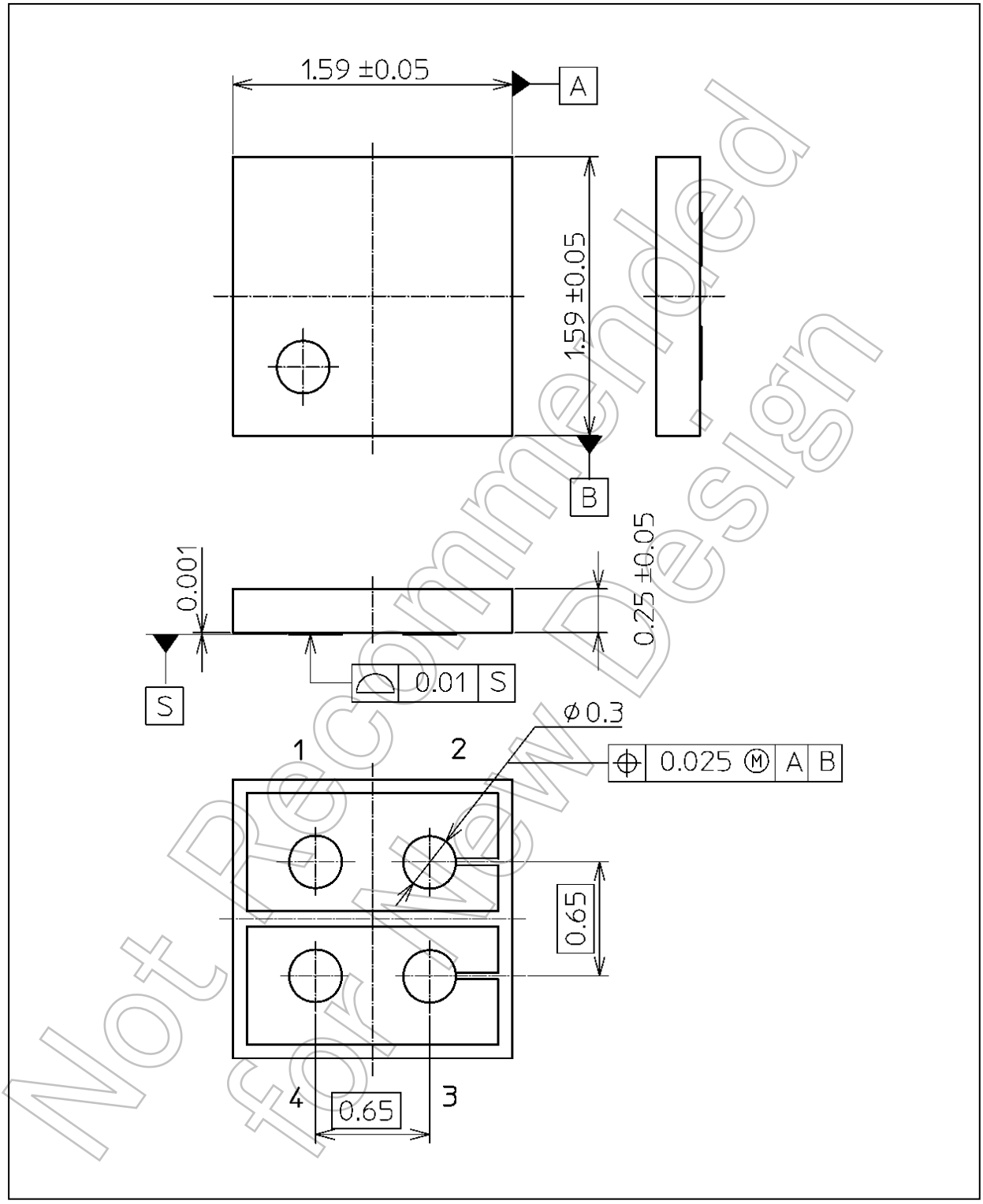
Package Dimensions

Unit: mm



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Weight: 0.00147 g (typ.)

Package Name(s)
TOSHIBA: 2-2W1S
Nickname: ChipLGA

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