Features

- 3000 Dhrystone 2.1 MIPS at 1.3 GHz
- Selectable Bus Clock (30 CPU Bus Dividers up to 28x)
- 13 Selectable Core-to-L3 Frequency Divisors
- Selectable MPx/60x Interface Voltage (1.8V, 2.5V)
- Selectable L3 Interface of 1.8V or 2.5V
- P_D Typical 12.6W at 1 GHz at V_{DD} = 1.3V; 8.3W at 1 GHz at V_{DD} = 1.1V, Full Operating Conditions
- Nap, Doze and Sleep Modes for Power Saving
- Superscalar (Four Instructions Fetched Per Clock Cycle)
- 4 GB Direct Addressing Range
- Virtual Memory: 4 Hexabytes (2^{52})
- 64-bit Data and 36-bit Address Bus Interface
- Integrated L1: 36 KB Instruction and 32 KB Data Cache
- Integrated L2: 512 KB
- 11 Independent Execution Units and Three Register Files
- Write-back and Write-through Operations
- f_{INT} Max = 1 GHz (1.2 GHz to be Confirmed)
- f_{BUS} Max = 133 MHz/166 MHz

Description

The PC7457 is implementations of the PowerPC® microprocessor family of reduced instruction set computer (RISC) microprocessors. This document describes pertinent electrical and physical characteristics of the PC7457.

The PC7457 is the fourth implementation of the fourth generation (G4) microprocessors from Freescale. The PC7457 implements the full PowerPC 32-bit architecture and is targeted at networking and computing systems applications. The PC7457 consists of a processor core, a 512 Kbyte L2, and an internal L3 tag and controller which support a glueless backside L3 cache through a dedicated high-bandwidth interface.

The core is a high-performance superscalar design supporting a double-precision floating-point unit and a SIMD multimedia unit. The memory storage subsystem supports the MPX bus interface to main memory and other system resources. The L3 interface supports 1, 2, or 4M bytes of external SRAM for L3 cache and/or private memory data. For systems implementing 4M bytes of SRAM, a maximum of 2M bytes may be used as cache; the remaining 2M bytes must be private memory.

Note that the PC7457 is a footprint-compatible, drop-in replacement in a PC7455 application if the core power supply is 1.3V.

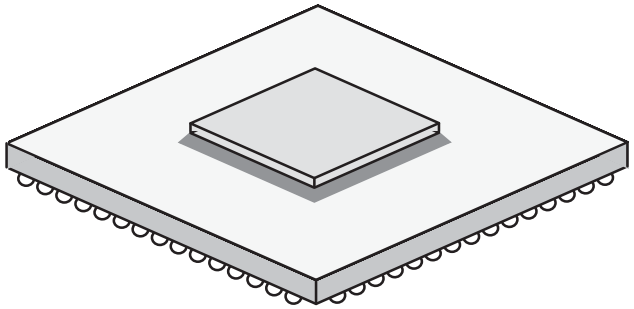
PowerPC 7457 RISC Microprocessor

PC7457

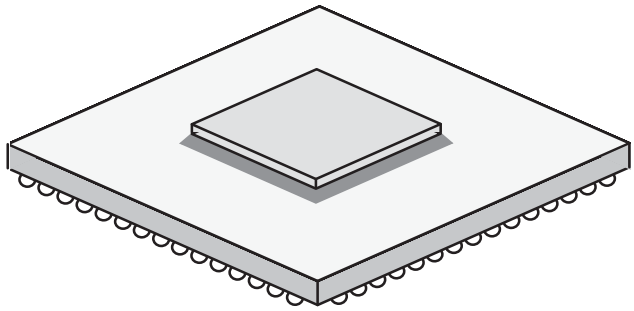
Rev. 5345D–HIREL–07/06

Screening

- CBGA Upscreenings Based on Atmel Standards
- Full Military Temperature Range (T_J = -55° C, +125° C), Industrial Temperature Range (T_J = -40° C, +110° C)
- HCTE Package for the 7457



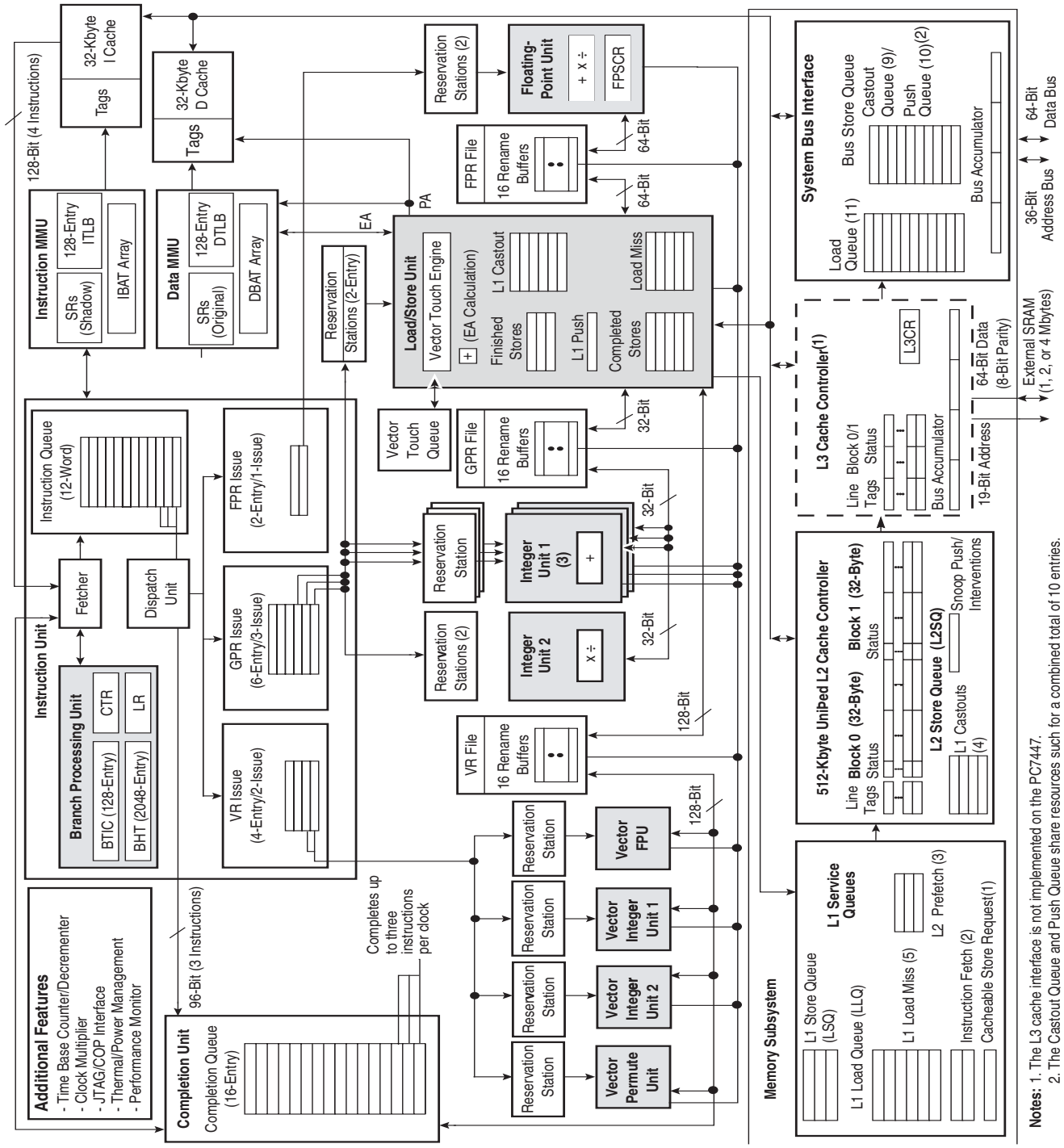
G suffix
CBGA 483
Ceramic Ball Grid Array



GH suffix
HITCE 483
Ceramic Ball Grid Array

1. Block Diagram

Figure 1-1. PC7457 Microprocessor Block Diagram



Notes: 1. The L3 cache interface is not implemented on the PC7447.
2. The Castout Queue and Push Queue share resources such for a combined total of 10 entries. The Castout Queue itself is limited to 9 entries, ensuring 1 entry will be available for a push.

2. General Parameters

Table 2-1 provides a summary of the general parameters of the PC7457.

Table 2-1. Device Parameters

Parameter	Description
Technology	0.13 µm CMOS, nine-layer metal
Die size	9.1 mm × 10.8 mm
Transistor count	58 million
Logic design	Fully-static
Packages	PC7447: surface mount 360 ceramic ball grid array (CBGA) PC7457: surface mount 483 ceramic ball grid array (CBGA) + HiTCE CBGA
Core power supply	1.3V ±500 mV DC nominal or 1.1V ±50 mV (nominal, see "Recommended Operating Conditions(1)" on page 12
I/O power supply	1.8V ±5% DC, or 2.5V ±5% for recommended operating conditions

3. Overview

This section summarizes features of the PC7457 implementation of the PowerPC architecture. Major features of the PC7457 are as follows:

- High-performance, superscalar microprocessor
  - As many as 4 instructions can be fetched from the instruction cache at a time
  - As many as 3 instructions can be dispatched to the issue queues at a time
  - As many as 12 instructions can be in the instruction queue (IQ)
  - As many as 16 instructions can be at some stage of execution simultaneously
  - Single-cycle execution for most instructions
  - One instruction per clock cycle throughput for most instructions
  - Seven-stage pipeline control

- Eleven independent execution units and three register files
  - Branch processing unit (BPU) features static and dynamic branch prediction

    128-entry (32-set, four-way set-associative) branch target instruction cache (BTIC), a cache of branch instructions that have been encountered in branch/loop code sequences. If a target instruction is in the BTIC, it is fetched into the instruction queue a cycle sooner than it can be made available from the instruction cache. Typically, a fetch that hits the BTIC provides the first four instructions in the target stream

    2048-entry branch history table (BHT) with two bits per entry for four levels of prediction – not-taken, strongly not-taken, taken, and strongly taken

    Up to three outstanding speculative branches

    Branch instructions that don't update the count register (CTR) or link register (LR) are often removed from the instruction stream

Eight-entry link register stack to predict the target address of Branch Conditional to Link Register (BCLR) instructions

– Four integer units (IUs) that share 32 GPRs for integer operands

Three identical IUs (IU1a, IU1b, and IU1c) can execute all integer instructions except multiply, divide, and move to/from special-purpose register instructions

IU2 executes miscellaneous instructions including the CR logical operations, integer multiplication and division instructions, and move to/from special-purpose register instructions

– Five-stage FPU and a 32-entry FPR file

Fully IEEE 754-1985-compliant FPU for both single- and double-precision operations

Supports non-IEEE mode for time-critical operations

Hardware support for denormalized numbers

Thirty-two 64-bit FPRs for single- or double-precision operands

– Four vector units and 32-entry vector register file (VRs)

Vector permute unit (VPU)

Vector integer unit 1 (VIU1) handles short-latency AltiVec integer instructions, such as vector add instructions (vaddsbs, vaddshs, and vaddsws, for example)

Vector integer unit 2 (VIU2) handles longer-latency AltiVec integer instructions, such as vector multiply add instructions (vmhaddshs, vmhraddshs, and vmladduhm, for example)

Vector floating-point unit (VFPU)

– Three-stage load/store unit (LSU)

Supports integer, floating-point, and vector instruction load/store traffic

Four-entry vector touch queue (VTQ) supports all four architected AltiVec data stream operations

Three-cycle GPR and AltiVec load latency (byte, half-word, word, vector) with one-cycle throughput

Four-cycle FPR load latency (single, double) with one-cycle throughput

No additional delay for misaligned access within double-word boundary

Dedicated adder calculates effective addresses (EAs)

Supports store gathering

Performs alignment, normalization, and precision conversion for floating-point data

Executes cache control and TLB instructions

Performs alignment, zero padding, and sign extension for integer data

Supports hits under misses (multiple outstanding misses)

Supports both big- and little-endian modes, including misaligned little-endian accesses

- Three issue queues FIQ, VIQ, and GIQ can accept as many as one, two, and three instructions, respectively, in a cycle. Instruction dispatch requires the following:
  - Instructions can be dispatched only from the three lowest IQ entries – IQ0, IQ1, and IQ2
  - A maximum of three instructions can be dispatched to the issue queues per clock cycle
  - Space must be available in the CQ for an instruction to dispatch (this includes instructions that are assigned a space in the CQ but not in an issue queue)
- Rename buffers
  - 16 GPR rename buffers
  - 16 FPR rename buffers
  - 16 VR rename buffers
- Dispatch unit
  - Decode/dispatch stage fully decodes each instruction
- Completion unit
  - The completion unit retires an instruction from the 16-entry completion queue (CQ) when all instructions ahead of it have been completed, the instruction has finished execution, and no exceptions are pending
  - Guarantees sequential programming model (precise exception model)
  - Monitors all dispatched instructions and retires them in order
  - Tracks unresolved branches and flushes instructions after a mispredicted branch
  - Retires as many as three instructions per clock cycle
- Separate on-chip L1 Instruction and data caches (Harvard Architecture)
  - 32 Kbyte, eight-way set-associative instruction and data caches
  - Pseudo least-recently-used (PLRU) replacement algorithm
  - 32-byte (eight-word) L1 cache block
  - Physically indexed/physical tags
  - Cache write-back or write-through operation programmable on a per-page or per-block basis

  - Instruction cache can provide four instructions per clock cycle; data cache can provide four words per clock cycle
  - Caches can be disabled in software
  - Caches can be locked in software
  - MESI data cache coherency maintained in hardware
  - Separate copy of data cache tags for efficient snooping
  - Parity support on cache and tags
  - No snooping of instruction cache except for icbi instruction
  - Data cache supports AltiVec LRU and transient instructions
  - Critical double- and/or quad-word forwarding is performed as needed. Critical quad-word forwarding is used for AltiVec loads and instruction fetches. Other accesses use critical double-word forwarding
- Level 2 (L2) cache interface
  - On-chip, 512 Kbyte, eight-way set-associative unified instruction and data cache
  - Fully pipelined to provide 32 bytes per clock cycle to the L1 caches
  - A total nine-cycle load latency for an L1 data cache miss that hits in L2
  - PLRU replacement algorithm
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - 64-byte, two-sectored line size
  - Parity support on cache
- Level 3 (L3) cache interface (not implemented on PC7447)
  - Provides critical double-word forwarding to the requesting unit
  - Internal L3 cache controller and tags
  - External data SRAMs
  - Support for 1, 2, and 4M bytes (MB) total SRAM space
  - Support for 1 or 2 MB of cache space
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - 64-byte (1 MB) or 128-byte (2 MB) sectored line size
  - Private memory capability for half (1 MB minimum) or all of the L3 SRAM space for a total of 1-, 2-, or 4-MB of private memory
  - Supports MSUG2 dual data rate (DDR) synchronous Burst SRAMs, PB2 pipelined synchronous Burst SRAMs, and pipelined (register-register) Late Write synchronous Burst SRAMs
  - Supports parity on cache and tags
  - Configurable core-to-L3 frequency divisors
  - 64-bit external L3 data bus sustains 64-bit per L3 clock cycle
- Separate memory management units (MMUs) for Instructions and data
  - 52-bit virtual address; 32- or 36-bit physical address
  - Address translation for 4 Kbyte pages, variable-sized blocks, and 256M bytes segments

  - Memory programmable as write-back/write-through, caching-inhibited/caching-allowed, and memory coherency enforced/memory coherency not enforced on a page or block basis
  - Separate IBATs and DBATs (eight each) also defined as SPRs
  - Separate instruction and data translation lookaside buffers (TLBs)
    Both TLBs are 128-entry, two-way set-associative, and use LRU replacement algorithm
    TLBs are hardware- or software-reloadable (that is, on a TLB miss a page table search is performed in hardware or by system software)

- Efficient data flow
  - Although the VR/LSU interface is 128 bits, the L1/L2/L3 bus interface allows up to 256 bits
  - The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs
  - L2 cache is fully pipelined to provide 256 bits per processor clock cycle to the L1 cache
  - As many as eight outstanding, out-of-order, cache misses are allowed between the L1 data cache and L2/L3 bus
  - As many as 16 out-of-order transactions can be present on the MPX bus
  - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed)
  - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - Hardware-enforced, MESI cache coherency protocols for data cache
  - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - 1.6V processor core
  - The following three power-saving modes are available to the system:

    Nap—Instruction fetching is halted. Only those clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a QREQ/QACK processor-system handshake protocol

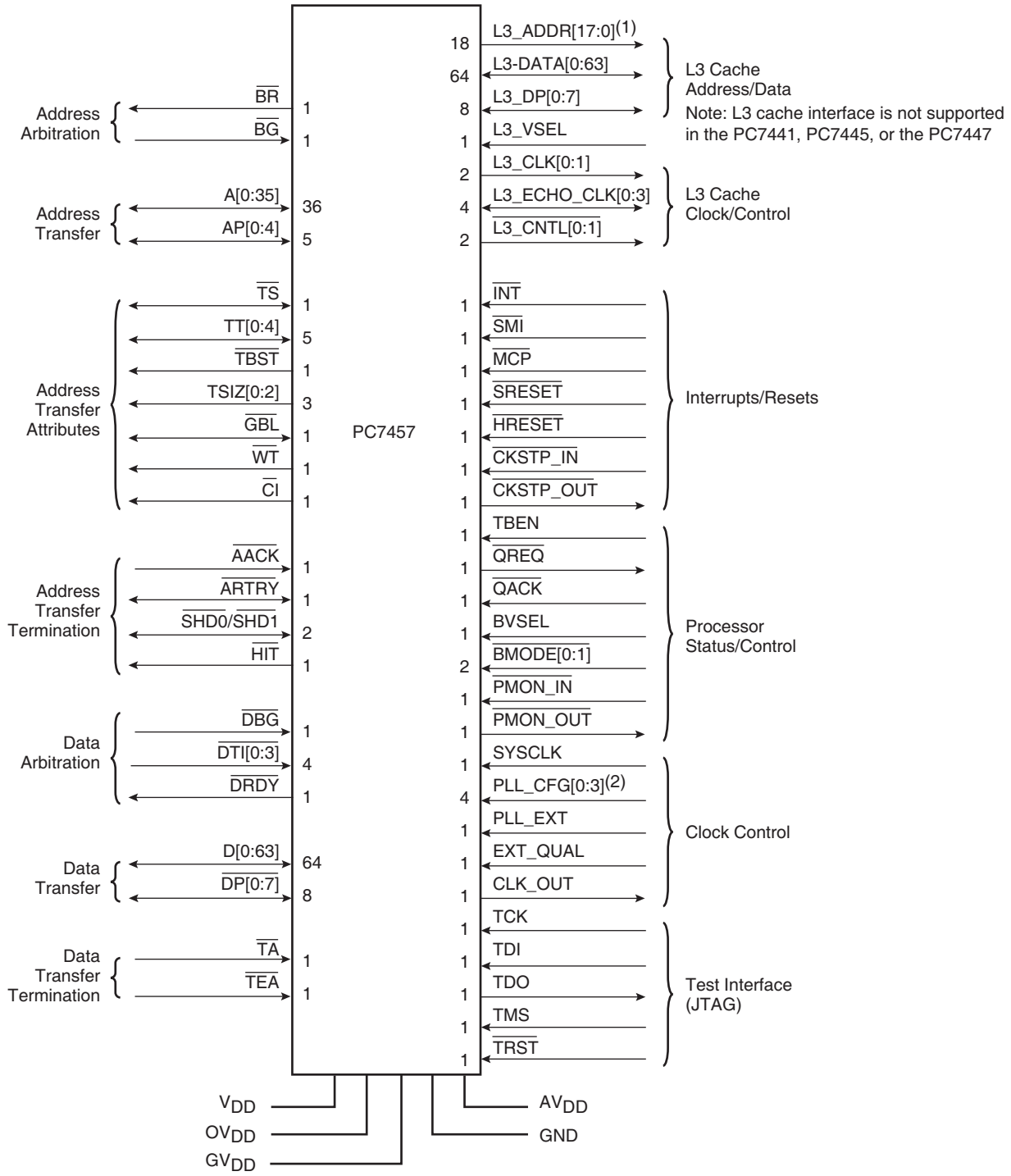
    Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled

    Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed on exiting the deep sleep state

  - Thermal management facility provides software-controllable thermal management. Thermal management is performed through the use of three supervisor-level registers and a PC7457-specific thermal management exception
  - Instruction cache throttling provides control of instruction fetching to limit power consumption
- Performance monitor can be used to help debug system designs and improve software efficiency
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
  - Array built-in self test (ABIST) – factory test only
- Reliability and serviceability
  - Parity checking on system bus and L3 cache bus
  - Parity checking on the L2 and L3 cache tag arrays

4. Signal Description

Figure 4-1. PC7457 Microprocessor Signal Groups



Notes: 1. For the PC7457, there are 19 L3_ADDR signals, (L3_ADDR[0:18].
2. For the PC7447 and PM7457, there are 5 PLL_CFG signals, (PLL_CFG[0:4].

5. Detailed Specification

This specification describes the specific requirements for the microprocessor PC7457 in compliance with Atmel standard screening.

6. Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics
2. MIL-PRF-38535: Appendix A: General specifications for microcircuits

The microcircuits are in accordance with the applicable documents and as specified herein.

6.1 Design and Construction

6.1.1 Terminal Connections

Depending on the package, the terminal connections are as shown in "Recommended Operating Conditions(1)" on page 12 and Figure 4-1 on page 10.

6.1.2 Absolute Maximum Ratings(1)

Symbol	Characteristic		Maximum Value	Unit
V_{DD}(2)	Core supply voltage		-0.3 to 1.60	V
AV_{DD}(2)	PLL supply voltage		-0.3 to 1.60	V
OV_{DD}(3)(4)	Processor bus supply voltage	BVSEL = 0	-0.3 to 1.95	V
OV_{DD}(3)(5)		BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	-0.3 to 2.7	V
GV_{DD}(3)(6)	L3 bus supply voltage	L3VSEL = ¬$\overline{\text{HRESET}}$	-0.3 to 1.65	V
GV_{DD}(3)(7)		L3VSEL = 0	-0.3 to 1.95	V
GV_{DD}(3)(8)		L3VSEL = $\overline{\text{HRESET}}$ or GV_{DD}	-0.3 to 2.7	V
V_{IN}(9)(10)	Input voltage	Processor bus	-0.3 to OV_{DD} + 0.3	V
V_{IN}(9)(10)		L3 bus	-0.3 to GV_{DD} + 0.3	V
V_{IN}		JTAG signals	-0.3 to OV_{DD} + 0.3	V
T_{STG}	Storage temperature range		-55 to 150	°C

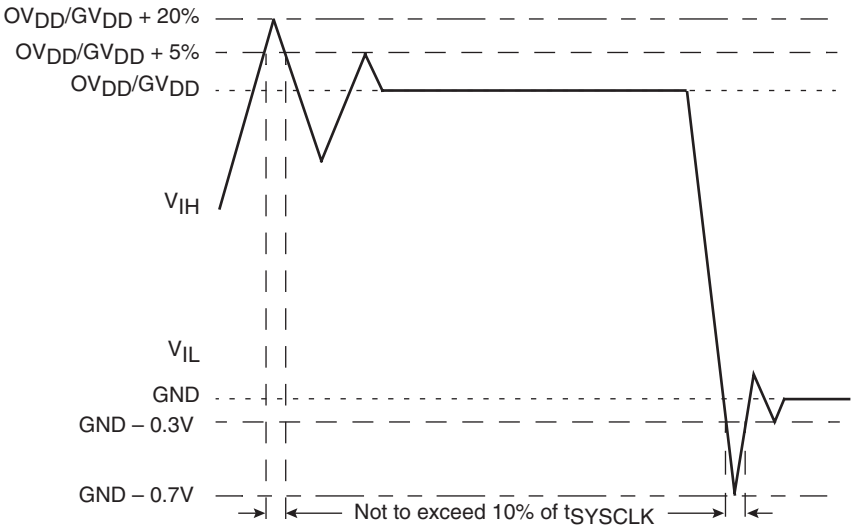
Notes:
1. Functional and tested operating conditions are given in "Recommended Operating Conditions(1)" on page 12. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: V_{DD}/AV_{DD} must not exceed OV_{DD}/GV_{DD} by more than 1V during normal operation; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. Caution: OV_{DD}/GV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2V during normal operation; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. BVSEL must be set to 0, such that the bus is in 1.8V mode.
5. BVSEL must be set to $\overline{\text{HRESET}}$ or 1, such that the bus is in 2.5V mode.
6. L3VSEL must be set to ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), such that the bus is in 1.5V mode.
7. L3VSEL must be set to 0, such that the bus is in 1.8V mode.
8. L3VSEL must be set to $\overline{\text{HRESET}}$ or 1, such that the bus is in 2.5V mode.
9. Caution: V_{IN} must not exceed OV_{DD} or GV_{DD} by more than 0.3V at any time including during power-on reset.
10. V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 6-1.

6.1.3 Recommended Operating Conditions[1]

Symbol	Characteristic		Recommended Value		Unit
			Min	Max	
V_{DD}	Core supply voltage		1.3V ±50 mV or 1.1V ±50 mV		V
AV_{DD}[2]	PLL supply voltage		1.3V ±50 mV or 1.1V ±50 mV		V
OV_{DD}	Processor bus supply voltage	BVSEL = 0	1.8V ±5%		V
OV_{DD}		BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	2.5V ±5%		V
GV_{DD}	L3 bus supply voltage	L3VSEL = 0	1.8V ±5%		V
GV_{DD}		L3VSEL = $\overline{\text{HRESET}}$ or GV_{DD}	2.5V ±5%		V
GV_{DD}[3]		L3VSEL = ¬$\overline{\text{HRESET}}$	1.5V ±5%		V
V_{IN}	Input voltage	Processor bus	GND	OV_{DD}	V
V_{IN}		L3 bus	GND	GV_{DD}	V
V_{IN}		JTAG signals	GND	OV_{DD}	V
T_J	Die-junction temperature		-55	125	°C

Notes:
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. This voltage is the input to the filter discussed in Section "PLL Power Supply Filtering" on page 50 and not necessarily the voltage at the AV_{DD} pin which may be reduced from V_{DD} by the filter.
3. ¬$\overline{\text{HRESET}}$ is the inverse of $\overline{\text{HRESET}}$.

Figure 6-1. Overshoot/Undershoot Voltage



The PC7457 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The PC7457 core voltage must always be provided at nominal 1.3V (see "Recommended Operating Conditions[1]" on page 12 for actual recommended core voltage). Voltage to the L3 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 6-1. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal $\overline{\text{HRESET}}$. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or GV_{DD} power pins.

Table 6-1. Input Threshold Voltage Setting

BVSEL Signal	Processor Bus Input Threshold is Relative to:	L3VSEL Signal[1]	L3 Bus Input Threshold is Relative to:	Notes
0	1.8V	0	1.8V	(2)(3)
¬$\overline{\text{HRESET}}$	Not available	¬$\overline{\text{HRESET}}$	1.5V	(2)(4)
$\overline{\text{HRESET}}$	2.5V	$\overline{\text{HRESET}}$	2.5V	(2)
1	2.5V	1	2.5V	(2)

Notes:
1. Not implemented on PC7447.
2. Caution: The input threshold selection must agree with the OV_{DD}/GV_{DD} voltages supplied. See notes in "Absolute Maximum Ratings[1]" on page 11.
3. If used, pull-down resistors should be less than 250Ω
4. Applicable to L3 bus interface only. ¬$\overline{\text{HRESET}}$ is the inverse of $\overline{\text{HRESET}}$.

6.2 Thermal Characteristics

6.2.1 Package Characteristics

Table 6-2. Package Thermal Characteristics[1]

Symbol	Characteristic	Value		Unit
		PC7447 CBGA	PC7457 CBGA	
$R_{\theta JA}$[2][3]	Junction-to-ambient thermal resistance, natural convection	22	20	°C/W
$R_{\theta JMA}$[2][4]	Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	14	14	°C/W
$R_{\theta JMA}$[2][4]	Junction-to-ambient thermal resistance, 200 ft./min. airflow, single-layer (1s) board	16	15	°C/W
$R_{\theta JMA}$[2][4]	Junction-to-ambient thermal resistance, 200 ft./min. airflow, four-layer (2s2p) board	11	11	°C/W
$R_{\theta JB}$[5]	Junction-to-board thermal resistance	6	6	°C/W
$R_{\theta JC}$[6]	Junction-to-case thermal resistance	< 0.1	< 0.1	°C/W
	Coefficient of thermal expansion	6.8	6.8	ppm/°C

Notes:
1. See "Thermal Management Information" on page 15 for more details about thermal management.
2. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
3. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
4. Per JEDEC JESD51-6 with the board horizontal.
5. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
6. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.

6.2.2 Package Thermal Characteristics for HCTE

Table 6-3 provides the package thermal characteristics for the PC7457, HCTE.

Table 6-3. Package Thermal Characteristics for HCTE Package

Characteristic	Symbol	Value	Unit
		PC755 HCTE	
Junction-to-bottom of balls(1)	$R\theta_J$	3.9	°C/W
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board(1)(2)	$R\theta_{JMA}$	16.8	°C/W
Junction to board thermal resistance	$R\theta_{JB}$	7.6	°C/W

Notes: 1. Simulation, no convection air flow.
2. Per JEDEC JESD51-6 with the board horizontal

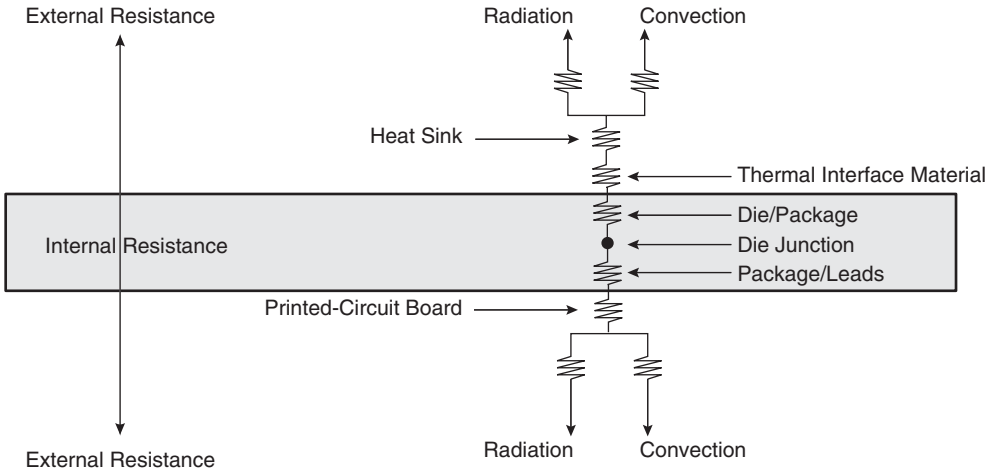
6.2.3 Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in Table 6-1 on page 13, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (actually top-of-die since silicon die is exposed) thermal resistance
- The die junction-to-ball thermal resistance

Figure 15-3 on page 55 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 6-2. C4 Package with Heat Sink Mounted to a Printed-Circuit Board



Note the internal versus external package resistance.

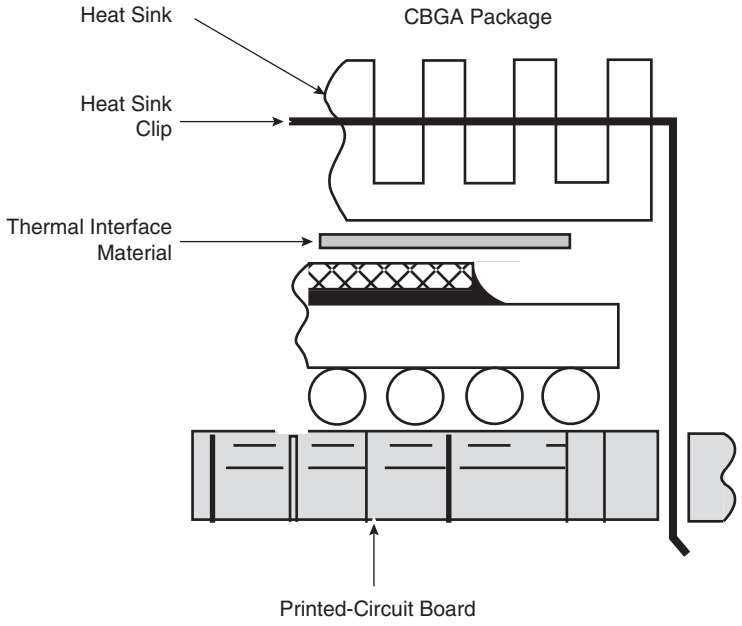
Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

6.2.4 Thermal Management Information

This section provides thermal management information for the ceramic ball grid array (CBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design – the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods – spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (see Figure 15-2 on page 52); however, due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. If a spring clip is used, the spring force should not exceed 10 pounds.

Figure 6-3. Package Exploded Cross-sectional View with Several Heat Sink Options



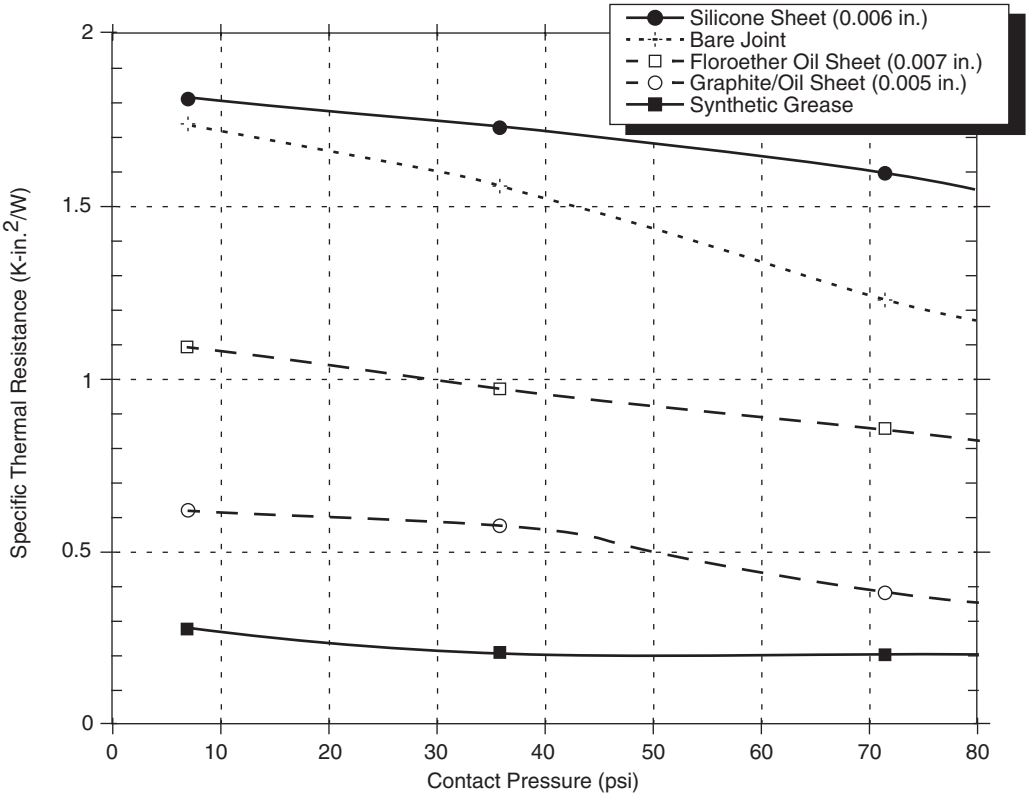
6.2.5 Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 6-3 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure.

The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 15-2 on page 52). Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure and is recommended due to the high power dissipation of the PC7457. Of course, the selection of any thermal interface material depends on many factors – thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.

Figure 6-4. Thermal Performance of Select Thermal Interface Material



6.2.5.1 *Heat Sink Selection Example*

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$T_J = T_I + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$

where:

T_J is the die-junction temperature
T_I is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
$R_{\theta JC}$ is the junction-to-case thermal resistance
$R_{\theta int}$ is the adhesive or interface material thermal resistance
$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance
P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_J) should be maintained less than the value specified in "Recommended Operating Conditions(1)" on page 12. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40° C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10° C.

The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 1.5° C/W. For example, assuming a Ta of 30° C, a Tr of 5° C, a CBGA package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 18.7W, the following expression for T_J is obtained:

Die-junction temperature: T_J = 30° C + 5° C + (0.1° C/W + 1.5° C/W + θ_{sa}) × 18.7W

For this example, a $R_{\theta sa}$ value of 2.1° C/W or less is required to maintain the die junction temperature below the maximum value of "Recommended Operating Conditions(1)" on page 12.

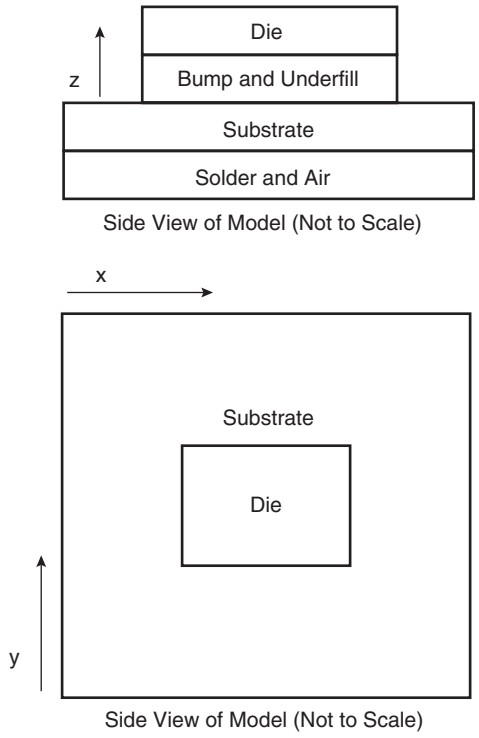
Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature – airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as system-level designs.

For system thermal modeling, the PC7447 and PC7457 thermal model is shown in Figure 6-2 on page 14. Four volumes will be used to represent this device. Two of the volumes, solder ball, and air and substrate, are modeled using the package outline size of the package. The other two, die, and bump and underfill, have the same size as the die. The silicon die should be modeled 9.64 × 11 × 0.74 mm with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as 9.64 × 11 × 0.69 mm (or as a collapsed volume) with orthotropic material properties: 0.6W/(m × K) in the xy-plane and 2W/(m × K) in the direction of the z-axis. The substrate volume is 25 × 25 × 1.2 mm (PC7447) or 29 × 29 × 1.2 mm (PC7457), and this volume has 18W/(m × K) isotropic conductivity. The solder ball and air layer is modeled with the same horizontal dimensions as the substrate and is 0.9 mm thick. It can also be modeled as a collapsed volume using orthotropic material properties: 0.034W/(m × K) in the xy-plane direction and 3.8W/(m × K) in the direction of the z-axis.

Figure 6-5. Recommended Thermal Model of PC7447 and PC7457

Conductivity	Value	Unit
Bump and Underfill		
k_x	0.6	W/(m x K)
k_y	0.6	
k_z	2	
Substrate		
k	18	
Solder Ball and Air		
k_x	0.034	
k_y	0.034	
k_z	3.8	



6.2.6 Power Consumption

Table 6-4. Power Consumption for PC7457

	Processor (CPU) Frequency				
Full-Power Mode	**600 MHz**	**1000 MHz**	**1000 MHz**	**1200 MHz**	**Unit**
Core Power Supply	1.1	1.1	1.3	1.3	
Typical(1)(2)	5.3	8.3	15.8	17.5	W
Maximum(1)(3)	7.9	11.5	22.0	24.2	W
Nap Mode					
Typical(1)(2)	1.3	1.3	5.2	5.2	W
Sleep Mode					
Typical(1)(2)	1.2	1.2	5.1	5.1	W
Deep Sleep Mode (PLL Disabled)					
Typical(1)(2)	1.1	1.1	5.0	5.0	W

Notes:
1. These values apply for all valid processor bus and L3 bus ratios. The values do not include I/O supply power (OV_{DD} and GV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} and GV_{DD} power is system dependent, but is typically < 5% of V_{DD} power. Worst case power consumption for AV_{DD} < 3 mW
2. Typical power is an average value measured at the nominal recommended VDD (see "Recommended Operating Conditions(1)" on page 12) and 65° C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz.

3. Maximum power is the average measured at nominal V_{DD} and maximum operating junction temperature (see "Recommended Operating Conditions(1)" on page 12) while running an entirely cache-resident, contrived sequence of instructions which keep all the execution units maximally busy.
4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.

7. Electrical Characteristics

7.1 Static Characteristics

Table 7-1 provides the DC electrical characteristics for the PC7457.

Table 7-1. DC Electrical Specifications (see "Recommended Operating Conditions(1)" on page 12)

Symbol	Characteristic		Nominal Bus Voltage(1)	Min	Max	Unit
V_{IH}(2)	Input high voltage (all inputs including SYSCLK)		1.5	$GV_{DD} \times 0.65$	$GV_{DD} + 0.3$	V
V_{IH}			1.8	$OV_{DD}/GV_{DD} \times 0.65$	$OV_{DD}/GV_{DD} + 0.3$	V
V_{IH}			2.5	1.7	$OV_{DD}/GV_{DD} + 0.3$	V
V_{IL}(2)(6)	Input low voltage (all inputs including SYSCLK)		1.5	-0.3	$GV_{DD} \times 0.35$	V
V_{IL}			1.8	-0.3	$OV_{DD}/GV_{DD} \times 0.35$	V
V_{IL}			2.5	-0.3	0.7	V
I_{IN}(2)(3)	Input leakage current, $V_{IN} = GV_{DD}/OV_{DD}$		–	–	30	µA
I_{TSI}(2)(3)(4)	High-impedance (off-state) Leakage current, $V_{IN} = GV_{DD}/OV_{DD}$		–	–	30	µA
V_{OH}(6)	Output high voltage, $I_{OH} = -5$ mA		1.5	$OV_{DD}/GV_{DD} - 0.45$	–	V
V_{OH}			1.8	$OV_{DD}/GV_{DD} - 0.45$	–	V
V_{OH}			2.5	1.8	–	V
V_{OL}(6)	Output low voltage, $I_{OL} = 5$ mA		1.5	–	0.45	V
V_{OL}			1.8	–	0.45	V
V_{OL}			2.5	–	0.6	V
C_{IN}	Capacitance, $V_{IN} = 0V$, f = 1 MHz	L3 interface(5)	–	–	9.5	pF
		All other inputs(5)		–	8.0	pF

Notes:
1. Nominal voltages; see "Recommended Operating Conditions(1)" on page 12 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while GV_{DD} is the reference for the L3 bus signals.
3. Excludes test signals and IEEE 1149.1 boundary scan (JTAG) signals.
4. The leakage is measured for nominal OV_{DD}/GV_{DD} and V_{DD}, or both OV_{DD}/GV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or -5%).
5. Capacitance is periodically sampled rather than 100% tested.
6. Applicable to L3 bus interface only

7.2 Dynamic Characteristics

This section provides the AC electrical characteristics for the PC7457. After fabrication, functional parts are sorted by maximum processor core frequency as shown in section “Clock AC Specifications” and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency; See “Ordering Information” on page 59.

7.2.1 Clock AC Specifications

Table 7-2 provides the clock AC timing specifications as defined in Figure 7-1 and represents the tested operating frequencies of the devices. The maximum system bus frequency, f_{SYSCLK}, given in Table 7-2 is considered a practical maximum in a typical single-processor system. The actual maximum SYSCLK frequency for any application of the PC7457 will be a function of the AC timings of the PC7457, the AC timings for the system controller, bus loading, printed-circuit board topology, trace lengths, and so forth, and may be less than the value given in Table 7-2.

Table 7-2. Clock AC Timing Specifications (See “Recommended Operating Conditions(1)” on page 12)

		Maximum Processor Core Frequency						
		600 MHz		867 MHz		1000 MHz		
		V_{DD} = 1.1V		V_{DD} = 1.1V		V_{DD} = 1.1V		
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{CORE}(1)	Processor frequency	500	600	500	867	500	1000	MHz
f_{VCO}(1)	VCO frequency	1000	1200	1000	1733	1000	2000	MHz
f_{SYSCLK}(1)(2)	SYSCLK frequency	33	167	33	167	33	167	MHz
t_{SYSCLK}(2)	SYSCLK cycle time	6	30	6	30	6	30	ns
t_{KR}, t_{KF}(3)	SYSCLK rise and fall time	–	1	–	1	–	1	ns
t_{KHKL}/t_{SYSCLK}(4)	SYSCLK duty cycle measured at $OV_{DD}/2$	40	60	40	60	–	–	%
	SYSCLK jitter(5)(6)	–	150	–	150	–	–	ps
	Internal PLL relock time(7)	–	100	–	100	–	–	µs

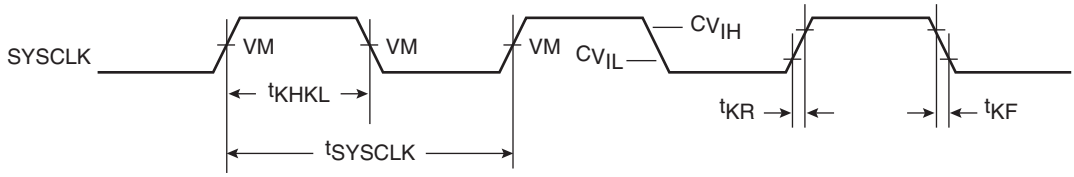
		Maximum Processor Core Frequency								
		867 MHz		1000 MHz		1200 MHz		1267 MHz		
		V_{DD} = 1.3V		V_{DD} = 1.3V		V_{DD} = 1.3V		V_{DD} = 1.3V		
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{CORE}(1)	Processor frequency	600	867	600	1000	600	1200	600	1267	MHz
f_{VCO}(1)	VCO frequency	1200	1733	1200	2000	1200	2400	1200	2534	MHz
f_{SYSCLK}(1)(2)	SYSCLK frequency	33	167	33	167	33	167	33	167	MHz
t_{SYSCLK}(2)	SYSCLK cycle time	6	30	6	30	6	30	6	30	ns
t_{KR}, t_{KF}(3)	SYSCLK rise and fall time	–	1	–	1	–	1	–	1	ns

Symbol	Characteristic	Maximum Processor Core Frequency								Unit
		867 MHz		1000 MHz		1200 MHz		1267 MHz		
		V_{DD} = 1.3V		V_{DD} = 1.3V		V_{DD} = 1.3V		V_{DD} = 1.3V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{KHKL}/t_{SYSCLK}[4]	SYSCLK duty cycle measured at $OV_{DD}/2$	40	60	40	60	40	60	40	60	%
	SYSCLK jitter[5][6]	–	±150	–	±150	–	±150	–	±150	ps
	Internal PLL relock time[7]	–	100	–	100	–	100	–	100	µs

Notes:
1. Caution: The SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency and PLL (VCO) frequency don't exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in "Core Clocks and PLL Configuration" on page 47 for valid PLL_CFG[0:4] settings
2. Assumes lightly-loaded, single-processor system.
3. Rise and fall times for the SYSCLK input measured from 0.4V to 1.4V.
4. Timing is guaranteed by design and characterization.
5. This represents total input jitter, short-term and long-term combined, and is guaranteed by design.
6. The SYSCLK driver's closed loop jitter bandwidth should be less than 1.5 MHz at -3 dB.
7. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 7-1 provides the SYSCLK input timing diagram.

Figure 7-1. SYSCLK Input Timing Diagram



VM = Midpoint Voltage ($OV_{DD}/2$)

7.2.2 Processor Bus AC Specifications

Table 7-3 provides the processor bus AC timing specifications for the PC7457 as defined in Figure 7-10 on page 33 and Figure 7-2 on page 23. Timing specifications for the L3 bus are provided in section "L3 Clock AC Specifications" on page 24.

Table 7-3. Processor Bus AC Timing Specifications[1] (at Recommended Operating Conditions, see page 12.)

Symbol[2]	Parameter	All Speed Grades			Unit
		V_{DD} = 1.1V	Min V_{DD} = 1.3V	Max	
	Input setup times:				
t_{AVKH}	A[0:35], AP[0:4]	2.0	1.8	–	
t_{DVKH}	D[0:63], DP[0:7]	2.0	1.8	–	
t_{IVKH}	$\overline{AACK}$, $\overline{ARTRY}$, $\overline{BG}$, $\overline{CKSTP\_IN}$, $\overline{DBG}$, DTI[0:3], $\overline{GBL}$, TT[0:3], $\overline{QACK}$, $\overline{TA}$, TBEN, $\overline{TEA}$, $\overline{TS}$, EXT_QUAL, $\overline{PMON\_IN}$, $\overline{SHD}$[0:1],	2.0	1.8	–	ns
t_{MVKH}[8]	BMODE[0:1], $\overline{BMODE}$[0:1], BVSEL, L3VSEL	2	1.8	–	
	Input hold times:				
t_{AXKH}	A[0:35], AP[0:4]	0	0	–	
t_{DXKH}	D[0:63], DP[0:7]	0	0	–	
t_{IXKH}	$\overline{AACK}$, $\overline{ARTRY}$, $\overline{BG}$, $\overline{CKSTP\_IN}$, $\overline{DBG}$, DTI[0:3], $\overline{GBL}$, TT[0:3], $\overline{QACK}$, $\overline{TA}$, TBEN, $\overline{TEA}$, $\overline{TS}$, EXT_QUAL, $\overline{PMON\_IN}$, $\overline{SHD}$[0:1]	0	0	–	ns
t_{MXKH}[8]	BMODE[0:1], $\overline{BMODE}$[0:1], BVSEL, L3VSEL	0	0	–	
	Output valid times: A[0:35], AP[0:4]				
t_{KHAV}	D[0:63], DP[0:7]	–	–	2	ns
t_{KHDV}	$\overline{AACK}$, $\overline{ARTRY}$, $\overline{BR}$, $\overline{CI}$, $\overline{CKSTP\_IN}$, $\overline{DRDY}$, DTI[0:3],	–	–	2	
t_{KHOV}	$\overline{GBL}$, $\overline{HIT}$, $\overline{PMON\_OUT}$, $\overline{QREQ}$, $\overline{TBST}$, TSIZ[0:2], TT[0:3], $\overline{TS}$, $\overline{SHD}$[0:1], $\overline{WT}$	–	–	2	
	Output hold times: A[0:35], AP[0:4]				
t_{KHAX}	D[0:63], DP[0:7]	0.5	0.5	–	ns
t_{KHDX}	$\overline{AACK}$, $\overline{ARTRY}$, $\overline{BR}$, $\overline{CI}$, $\overline{CKSTP\_IN}$, $\overline{DRDY}$, DTI[0:3],	0.5	0.5	–	
t_{KHOX}	$\overline{GBL}$, $\overline{HIT}$, $\overline{PMON\_OUT}$, $\overline{QREQ}$, $\overline{TBST}$, TSIZ[0:2], TT[0:3], $\overline{TS}$, $\overline{SHD}$[0:1], $\overline{WT}$	0.5	0.5	–	
t_{KHOE}	SYSCLK to output enable	0.5	0.5	–	ns
t_{KHOZ}	SYSCLK to output high impedance (all except $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$)	–	–	3.5	ns
t_{KHTSPZ}[3][4][5]	SYSCLK to $\overline{TS}$ high impedance after precharge	–	–	1	t_{SYSCLK}
t_{KHARP}[3][5][6][7]	Maximum delay to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ precharge	–	–	1	t_{SYSCLK}
t_{KHARPZ}[3][5][6][7]	SYSCLK to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ high impedance after precharge	–	–	2	t_{SYSCLK}

Notes: 1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50Ω load (see Figure 7-10 on page 33). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2. The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK (K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. According to the bus protocol, $\overline{TS}$ is driven only by the currently active bus master. It is asserted low then precharged high before returning to high impedance as shown in Figure 7-3 on page 24. The nominal precharge width for $\overline{TS}$ is 0.5 × t_{SYSCLK}, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{TS}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-impedance behavior is guaranteed by design.
5. Guaranteed by design and not tested.
6. According to the bus protocol, $\overline{ARTRY}$ can be driven by multiple bus masters through the clock period immediately following $\overline{AACK}$. Bus contention is not an issue because any master asserting $\overline{ARTRY}$ will be driving it low. Any master asserting it low in the first clock following $\overline{AACK}$ will then go to high impedance for one clock before precharging it high during the second cycle after the assertion of $\overline{AACK}$. The nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 7-3 on page 24 before the first opportunity for another master to assert $\overline{ARTRY}$. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
7. According to the MPX bus protocol, $\overline{SHD0}$ and $\overline{SHD1}$ can be driven by multiple bus masters beginning the cycle of $\overline{TS}$. Timing is the same as $\overline{ARTRY}$, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{SHD0}$ and $\overline{SHD1}$ is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
8. $\overline{BMODE}$[0:1] and BVSEL are mode select inputs and are sampled before and after $\overline{HRESET}$ negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. These inputs must remain stable after the second sample. See Figure 7-2 on page 23 for sample timing.

Figure 7-2. Mode Input Timing Diagram

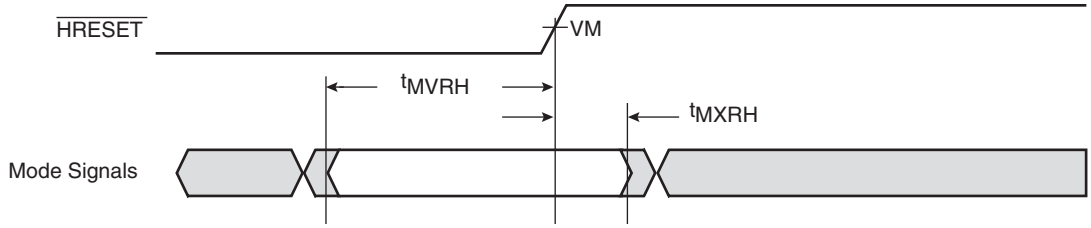
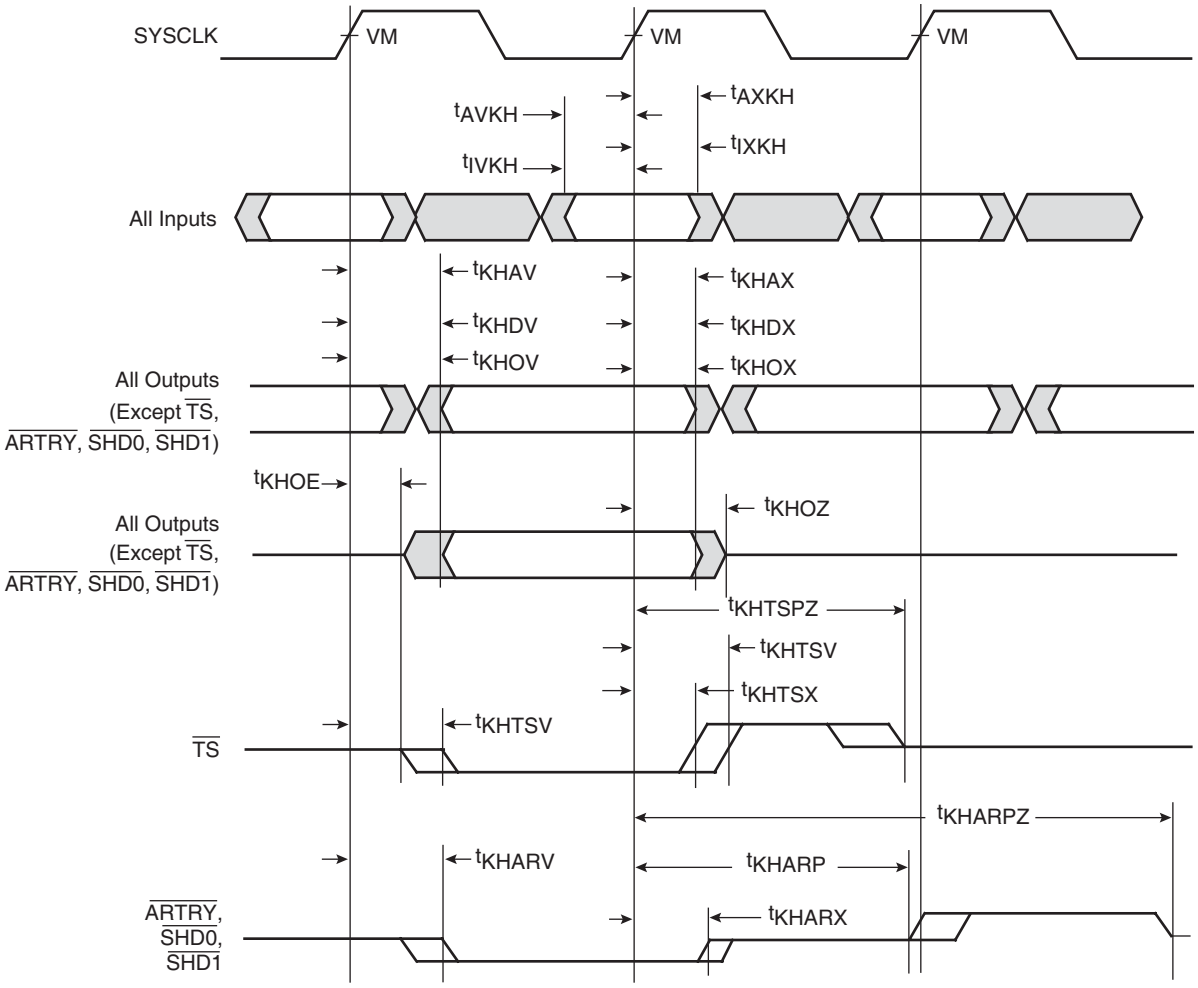


Figure 7-3 provides the input/output timing diagram for the PC7457.

Figure 7-3. Input/Output Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

7.2.3 L3 Clock AC Specifications

The L3_CLK frequency is programmed by the L3 configuration register core-to-L3 divisor ratio. See Table 15-1 on page 47 for example core and L3 frequencies at various divisors. Table 7-4 on page 25 provides the potential range of L3_CLK output AC timing specifications as defined in Figure 7-4 on page 26.

The maximum L3_CLK frequency is the core frequency divided by two. Given the high core frequencies available in the PC7457, however, most SRAM designs will be not be able to operate in this mode using current technology and, as a result, will select a greater core-to-L3 divisor to provide a longer L3_CLK period for read and write access to the L3 SRAMs. Therefore, the typical L3_CLK frequency shown in Table 7-4 is considered to be the practical maximum in a typical system. The maximum L3_CLK frequency for any application of the PC7457 will be a function of the AC timings of the PC7457, the AC timings for the SRAM, bus loading, and printed-circuit board trace length, and may be greater or less than the value given in Table 7-4.

Note that SYSCLK input jitter and L3_CLK[0:1] output jitter are already comprehended in the L3 bus AC timing specifications and do not need to be separately accounted for in an L3 AC timing analysis.

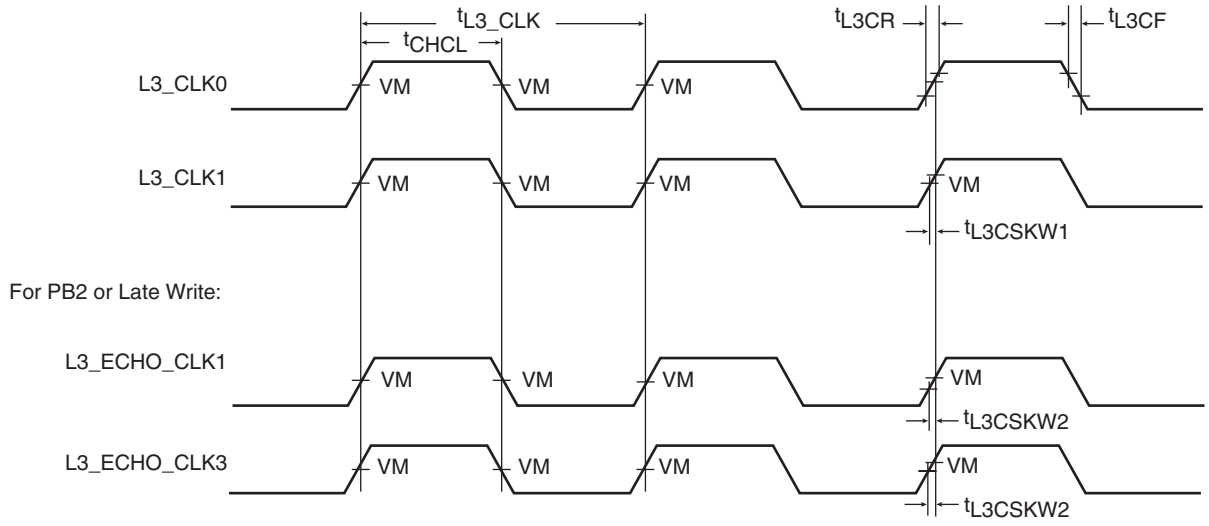
Clock skews, where applicable, do need to be accounted for in an AC timing analysis.Freescale is similarly limited by system constraints and cannot perform tests of the L3 interface on a socketed part on a functional tester at the maximum frequencies of Table 7-4. Therefore, functional operation and AC timing information are tested at core-to-L3 divisors which result in L3 frequencies at 250 MHz or lower.

Table 7-4. L3_CLK Output AC Timing Specifications at Recommended Operating Conditions (see page 12)[6]

Symbol	Parameter	All Speed Grades						Unit
		Min	Typical	Max	Min	Typical	Max	
f_{L3_CLK}[1]	L3 clock frequency	–	200		–	250	–	MHz
t_{L3_CLK}[1]	L3 clock cycle time	–	5	–	–	4	–	ns
t_{CHCL}/t_{L3_CLK}[2]	L3 clock duty cycle	–	50	–	–	50	–	%
$t_{L3CSKW1}$[3]	L3 clock output-to-output skew (L3_CLK0 to L3_CLK1)	–	–	100	–	–	100	ps
$t_{L3CSKW2}$[4]	L3 clock output-to-output skew (L3_CLK[0:1] to L3_ECHO_CLK[1:3])	–	–	100	–	–	100	ps
	L3 clock jitter[5]	–	–	±75	–	–	±75	ps

Notes:
1. The maximum L3 clock frequency (and minimum L3 clock period) will be system dependent. See "L3 Clock AC Specifications" on page 24 for an explanation that this maximum frequency is not functionally tested at speed by Freescale. The minimum L3 clock frequency and period are f_{SYSCLK} and t_{SYSCLK}, respectively.
2. The nominal duty cycle of the L3 output clocks is 50% measured at midpoint voltage.
3. Maximum possible skew between L3_CLK0 and L3_CLK1. This parameter is critical to the address and control signals which are common to both SRAM chips in the L3.
4. Maximum possible skew between L3_CLK0 and L3_ECHO_CLK1 or between L3_CLK1 and L3_ECHO_CLK3 for PB2 or Late Write SRAM. This parameter is critical to the read data signals because the processor uses the feedback loop to latch data driven from the SRAM, each of which drives data based on L3_CLK0 or L3_CLK1.
5. Guaranteed by design and not tested. The input jitter on SYSCLK affects L3 output clocks and the L3 address, data and control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L3 timing analysis. The clock-to-clock jitter shown here is uncertainty in the internal clock period caused by supply voltage noise or thermal effects. This is also comprehended in the AC timing specifications and need not be considered in the L3 timing analysis.
6. L3 I/O voltage mode must be configured by L3VSEL as described in Table 6-1 on page 13, and voltage supplied at GV_{DD} must match mode selected as specified in "Recommended Operating Conditions[1]" on page 12.

Figure 7-4. L3_CLK_OUT Output Timing Diagram

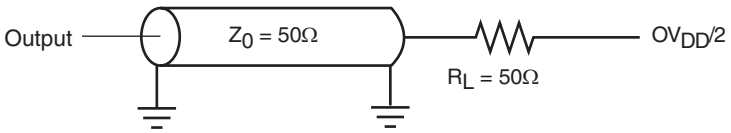


7.2.4 L3 Bus AC Specifications

The PC7457 L3 interface supports three different types of SRAM: source-synchronous, double data rate (DDR) MSUG2 SRAM, Late Write SRAMs, and pipeline burst (PB2) SRAMs. Each requires a different protocol on the L3 interface and a different routing of the L3 clock signals. The type of SRAM is programmed in L3CR[22:23] and the PC7457 then follows the appropriate protocol for that type. The designer must connect and route the L3 signals appropriately for each type of SRAM. Following are some observations about the L3 interface.

- The routing for the point-to-point signals (L3_CLK[0:1], L3DATA[0:63], L3DP[0:7], and L3_ECHO_CLK[0:3]) to a particular SRAM must be delay matched
- For 1M byte of SRAM, use L3_ADDR[16:0] (L3_ADDR[0] is LSB)
- For 2M bytes of SRAM, use L3_ADDR[17:0] (L3_ADDR[0] is LSB)
- No pull-up resistors are required for the L3 interface
- For high speed operations, L3 interface address and control signals should be a "T" with minimal stubs to the two loads; data and clock signals should be point-to-point to their single load. Figure 7-5 shows the AC test load for the L3 interface

Figure 7-5. AC Test Load for the L3 Interface



In general, if routing is short, delay-matched, and designed for incident wave reception and minimal reflection, there is a high probability that the AC timing of the PC7457 L3 interface will meet the maximum frequency operation of appropriately chosen SRAMs. This is despite the pessimistic, guard-banded AC specifications (see Table 7-6 on page 28, Table 7-7 on page 29, and Table 7-8 on page 31), the limitations of functional testers described in Section "L3 Clock AC Specifications" on page 24 and the uncertainty of clocks and signals which inevitably make worst-case critical path timing analysis pessimistic.

More specifically, certain signals within groups should be delay-matched with others in the same group while intergroup routing is less critical. Only the address and control signals are common to both SRAMs and additional timing margin is available for these signals. The double-clocked data signals are grouped with individual clocks as shown in Figure 7-6 on page 30 or Figure 7-8 on page 32, depending on the type of SRAM. For example, for the MSUG2 DDR SRAM (see Figure 7-6); L3DATA[0:31], L3DP[0:3], and L3_CLK[0] form a closely coupled group of outputs from the PC7457; while L3DATA[0:15], L3DP[0:1], and L3_ECHO_CLK[0] form a closely coupled group of inputs.

The PC7450 RISC Microprocessor Family User's Manual refers to logical settings called "sample points" used in the synchronization of reads from the receive FIFO. The computation of the correct value for this setting is system-dependent and is described in the PC7450 RISC Microprocessor Family User's Manual.

Three specifications are used in this calculation and are given in Table 7-5 on page 27. It is essential that all three specifications are included in the calculations to determine the sample points as incorrect settings can result in errors and unpredictable behavior. For more information, see the PC7450 RISC Microprocessor Family User's Manual.

Table 7-5. Sample Points Calculation Parameters

Symbol	Parameter	Max	Unit
t_{AC}	Delay from processor clock to internal_L3_CLK(1)	3/4	t_{L3_CLK}
t_{CO}	Delay from internal_L3_CLK to L3_CLK[n] output pins(2)	3	ns
t_{ECI}	Delay from L3_ECHO_CLK[n] to receive latch(3)	3	ns

Notes:
1. This specification describes a logical offset between the internal clock edge used to launch the L3 address and control signals (this clock edge is phase-aligned with the processor clock edge) and the internal clock edge used to launch the L3_CLK[n] signals. With proper board routing, this offset ensures that the L3_CLK[n] edge will arrive at the SRAM within a valid address window and provide adequate setup and hold time. This offset is reflected in the L3 bus interface AC timing specifications, but must also be separately accounted for in the calculation of sample points and, thus, is specified here.
2. This specification is the delay from a rising or falling edge on the internal_L3_CLK signal to the corresponding rising or falling edge at the L3CLK[n] pins.
3. This specification is the delay from a rising or falling edge of L3_ECHO_CLK[n] to data valid and ready to be sampled from the FIFO.

7.2.4.1 Effects of L3OHCR Settings on L3 Bus AC Specifications

The AC timing of the L3 interface can be adjusted using the L3 Output Hold Control Register (L3OCHR).

Each field controls the timing for a group of signals. The AC timing specifications presented herein represent the AC timing when the register contains the default value of 0x0000_0000. Incrementing a field delays the associated signals, increasing the output valid time and hold time of the affected signals. In the special case of delaying an L3_CLK signal, the net effect is to decrease the output valid and output hold times of all signals being latched relative to that clock signal. The amount of delay added is summarized in Table 7-6 on page 28. Note that these settings affect output timing parameters only and don't impact input timing parameters of the L3 bus in any way.

Table 7-6. Effect of L3OHCR Settings on L3 Bus AC Timing

Field name[1]	Affected Signals	Value	Output Valid Time		Output Hold Time		Unit	Notes
			Parameter Symbol[2]	Change[3]	Parameter Symbol[2]	Change[3]		
L3AOH	L3_ADDR[18:0], L3_CNTL[0:1]	0b00	t_{L3CHOV}	0	t_{L3CHOX}	0	ps	(4)
		0b01		+50		+50		
		0b10		+100		+100		
		0b11		+150		+150		
L3CLKn_OH	All signals latched by SRAM connected to L3_CLKn	0b000	t_{L3CHOV} t_{L3CHDV} t_{L3CLDV}	0	t_{L3CHOX} t_{L3CHDX} t_{L3CLDX}	0		(4)
		0b001		-50		-50		(5)
		0b010		-100		-100		(5)
		0b011		-150		-150		(5)
		0b100		-200		-200		(5)
		0b101		-250		-250		(5)
		0b110		-300		-300		(5)
		0b111		-350		-350		(5)
L3DOHn	L3_DATA[n:n + 7], L3_DP[n/8]	0b000	t_{L3CHDV} t_{L3CLDV}	0	t_{L3CHDX} t_{L3CLDX}	0		(4)
		0b001		+50		+50		
		0b010		+100		+100		
		0b011		+150		+150		
		0b100		+200		+200		
		0b101		+250		+250		
		0b111		+350		+350		
		0b111		+350		+350		

Notes:
1. Refer to the PC7450 RISC Microprocessor Family User's Manual for specific information regarding L3OHCR.
2. See Table 7-7 on page 29 and Table 7-8 on page 31 for more information.
3. Guaranteed by design; not tested or characterized.
4. Default value.
5. Increasing values of L3CLKn_OH delay the L3_CLKn signal, effectively decreasing the output valid and output hold times of all signals latched relative to that clock signal by the SRAM; see Figure 7-6 on page 30 and Figure 7-8 on page 32.

7.2.4.2 L3 Bus AC Specifications for DDR MSUG2 SRAMs

When using DDR MSUG2 SRAMs at the L3 interface, the parts should be connected as shown in Figure 7-6. Outputs from the PC7457 are actually launched on the edges of an internal clock phase-aligned to SYSCLK (adjusted for core and L3 frequency divisors). L3_CLK0 and L3_CLK1 are this internal clock output with 90° phase delay, so outputs are shown synchronous to L3_CLK0 and L3_CLK1. Output valid times are typically negative when referenced to L3_CLKn because the data is launched one-quarter period before L3_CLKn to provide adequate setup time at the SRAM after the delay-matched address, control, data, and L3_CLKn signals have propagated across the printed-wiring board.Inputs to the PC7457 are source-synchronous with the CQ clock generated by the DDR MSUG2 SRAMs. These CQ clocks are received on the L3_ECHO_CLKn inputs of the PC7457.

An internal circuit delays the incoming L3_ECHO_CLKn signal such that it is positioned within the valid data window at the internal receiving latches. This delayed clock is used to capture the data into these latches which comprise the receive FIFO. This clock is asynchronous to all other processor clocks. This latched data is subsequently read out of the FIFO synchronously to the processor clock. The time between writing and reading the data is set by the using the sample point settings defined in the L3CR register.Table 7-7 provides the L3 bus interface AC timing specifications for the configuration as shown in Figure 9, assuming the timing relationships shown in Figure 7-7 and the loading shown in Figure 7-5 on page 26.

Table 7-7. L3 Bus Interface AC Timing Specifications for MSUG2 at Recommended Operating Conditions (see page 12)

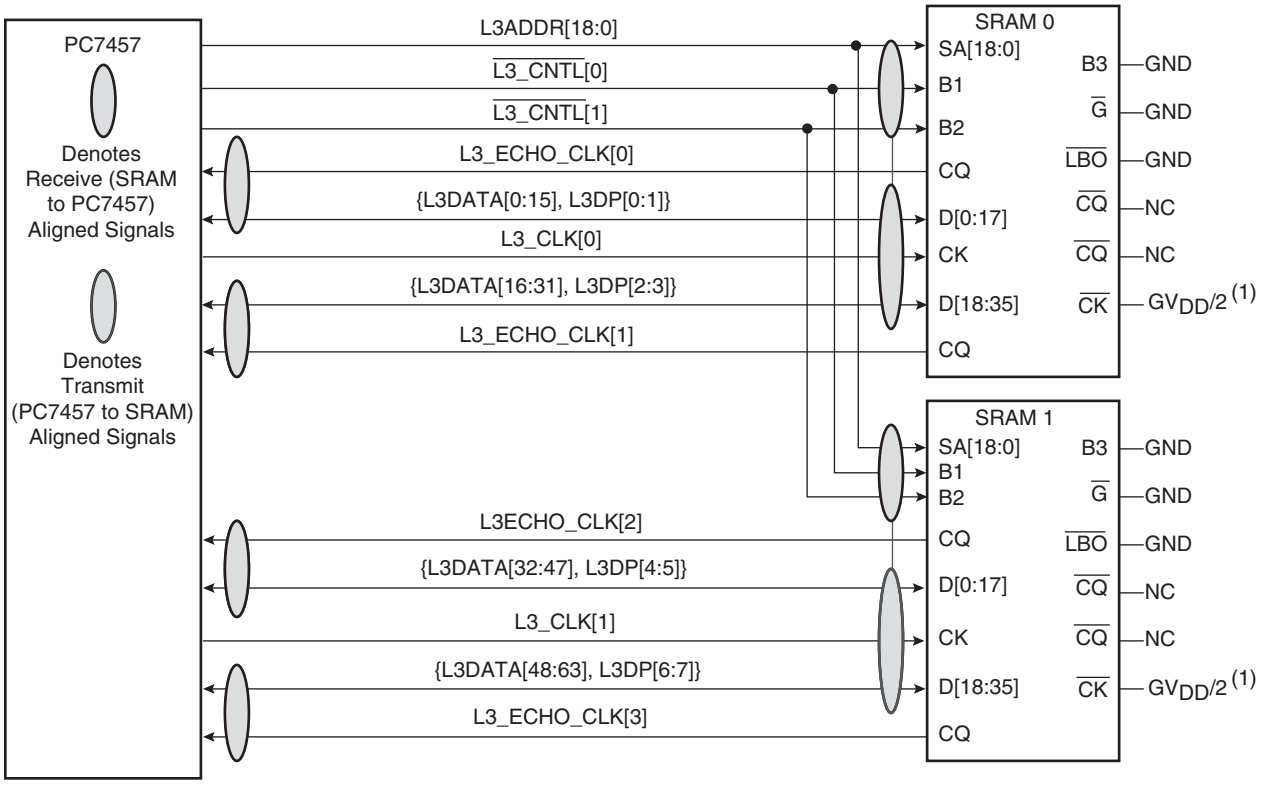
Symbol	Parameter	All Speed Grades[9]				Unit
		Min	Min	Max	Max	
t_{L3CR}, t_{L3CF}	L3_CLK rise and fall time[1]	–	0.75	–	0.75	ns
t_{L3DVEH}, t_{L3DVEL}	Setup times: Data and parity[2][3][4]	$(-t_{L3CLK}/4)$ + 0.90	–	$(-t_{L3CLK}/4)$ + 0.70	–	ns
t_{L3DXEH}, t_{L3DXEL}	Input hold times: Data and parity[2][4]	$(t_{L3CLK}/4)$ + 0.85	–	$(t_{L3CLK}/4)$ + 0.70	–	ns
t_{L3CHDV}, t_{L3CLDV}	Valid times: Data and parity[5][6][7][8]	–	$(-t_{L3CLK}/4)$ + 0.60	–	$(-t_{L3CLK}/4)$ + 0.50	ns
t_{L3CHOV}	Valid times: All other outputs[5][7][8]	–	$(t_{L3CLK}/4)$ + 0.65	–	$(t_{L3CLK}/4)$ + 0.65	ns
t_{L3CHDX}, t_{L3CLDX}	Output hold times: Data and parity[5][6][7][8]	$(t_{L3CLK}/4)$ - 0.60	–	$(t_{L3CLK}/4)$ - 0.50	–	ns
t_{L3CHOX}	Output hold times: All other outputs[5][7][8]	$(t_{L3CLK}/4)$ - 0.50	–	$(t_{L3CLK}/4)$ - 0.50	–	ns
t_{L3CLDZ}	L3_CLK to high impedance: Data and parity	–	$(-t_{L3CLK}/4)$ + 0.60	–	$(-t_{L3CLK}/4)$ + 0.60	ns
t_{L3CHOZ}	L3_CLK to high impedance: All other outputs	–	$(t_{L3CLK}/4)$ + 0.65	–	$(t_{L3CLK}/4)$ + 0.65	ns

Notes:
1. Rise and fall times for the L3_CLK output are measured from 20% to 80% of GV_{DD}.
2. For DDR, all input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising or falling edge of the input L3_ECHO_CLKn (see Figure 7-7 on page 30). Input timings are measured at the pins.
3. For DDR, the input data will typically follow the edge of L3_ECHO_CLKn as shown in Figure 7-7. For consistency with other input setup time specifications, this will be treated as negative input setup time.
4. $t_{L3\_CLK}/4$ is one-fourth the period of L3_CLKn. This parameter indicates that the PC7457 can latch an input signal that is valid for only a short time before and a short time after the midpoint between the rising and falling (or falling and rising) edges of L3_ECHO_CLKn at any frequency.
5. All output specifications are measured from the midpoint voltage of the rising (or for DDR write data, also the falling) edge of L3_CLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (see Figure 7-5 on page 26).
6. For DDR, the output data will typically lead the edge of L3_CLKn as shown in Figure 7-7 on page 30. For consistency with other output valid time specifications, this will be treated as negative output valid time.
7. $t_{L3\_CLK}/4$ is one-fourth the period of L3_CLKn. This parameter indicates that the specified output signal is actually launched by an internal clock delayed in phase by 90°. Therefore, there is a frequency component to the output valid and output hold times such that the specified output signal will be valid for approximately one L3_CLK period starting three-fourths of a clock prior to the edge on which the SRAM will sample it and ending one-fourth of a clock period after the edge it will be sampled.

8. Assumes default value of L3OHCR. See "Effects of L3OHCR Settings on L3 Bus AC Specifications" on page 27 for more information.
9. L3 I/O voltage mode must be configured by L3VSEL as described in Table 6-1 on page 13, and voltage supplied at GV_{DD} must match mode selected as specified in "Recommended Operating Conditions(1)" on page 12.

Figure 7-6 shows the typical connection diagram for the PC7457 interfaced to MSUG2 DDR SRAMs.

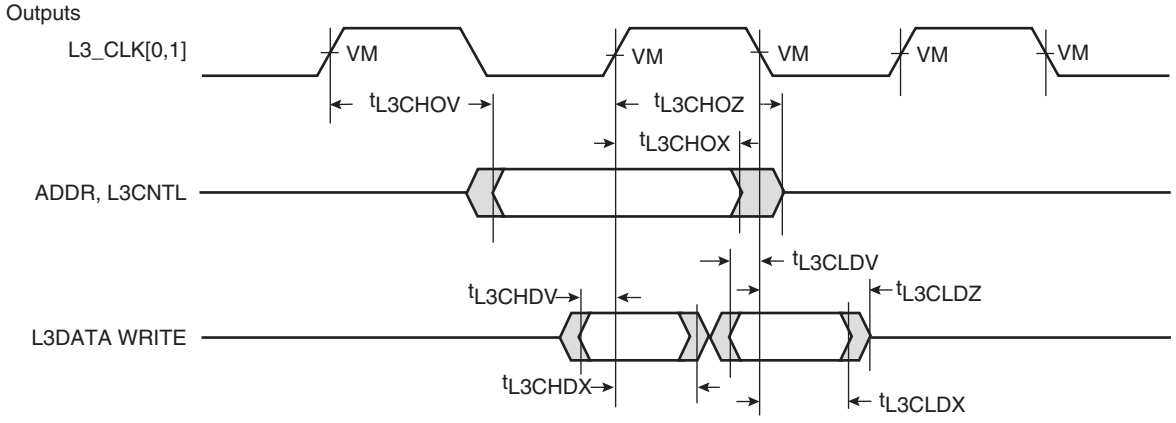
Figure 7-6. Typical Source Synchronous 4M bytes L3 Cache DDR Interface



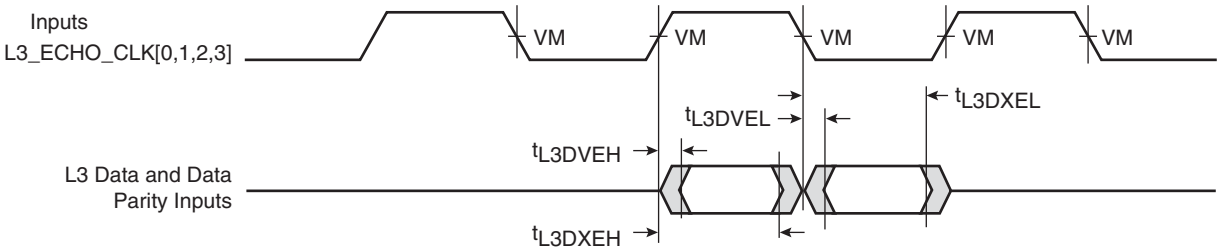
Note: 1. Or as recommended by SRAM manufacturer for single-ended clocking.

Figure 7-7 shows the L3 bus timing diagrams for the PC7457 interfaced to MSUG2 SRAMs.

Figure 7-7. L3 Bus Timing Diagrams for L3 Cache DDR SRAMs



Note: t_{L3CHDV} and t_{L3CLDV} as drawn here will be negative numbers, that is, output valid time will be time before the clock edge.



Notes: 1. t_{L3DVEH} and t_{L3DVEL} as drawn here will be negative numbers, that is, input setup time will be time after the clock edge.
2. VM = Midpoint Voltage ($GV_{DD}/2$)

7.2.5 L3 Bus AC Specifications for PB2 and Late Write SRAMs

When using PB2 or Late Write SRAMs at the L3 interface, the parts should be connected as shown in Figure 7-8 on page 32. These SRAMs are synchronous to the PC7457; one L3_CLKn signal is output to each SRAM to latch address, control, and write data. Read data is launched by the SRAM synchronous to the delayed L3_CLKn signal it received. The PC7457 needs a copy of that delayed clock which launched the SRAM read data to know when the returning data will be valid. Therefore, L3_ECHO_CLK1 and L3_ECHO_CLK3 must be routed halfway to the SRAMs and returned to the PC7457 inputs L3_ECHO_CLK0 and L3_ECHO_CLK2, respectively. Thus, L3_ECHO_CLK0 and L3_ECHO_CLK2 are phase-aligned with the input clock received at the SRAMs. The PC7457 will latch the incoming data on the rising edge of L3_ECHO_CLK0 and L3_ECHO_CLK2.Table 7-8 provides the L3 bus interface AC timing specifications for the configuration shown in Figure 7-8, assuming the timing relationships of Figure 7-9 and the loading of Figure 7-5 on page 26.

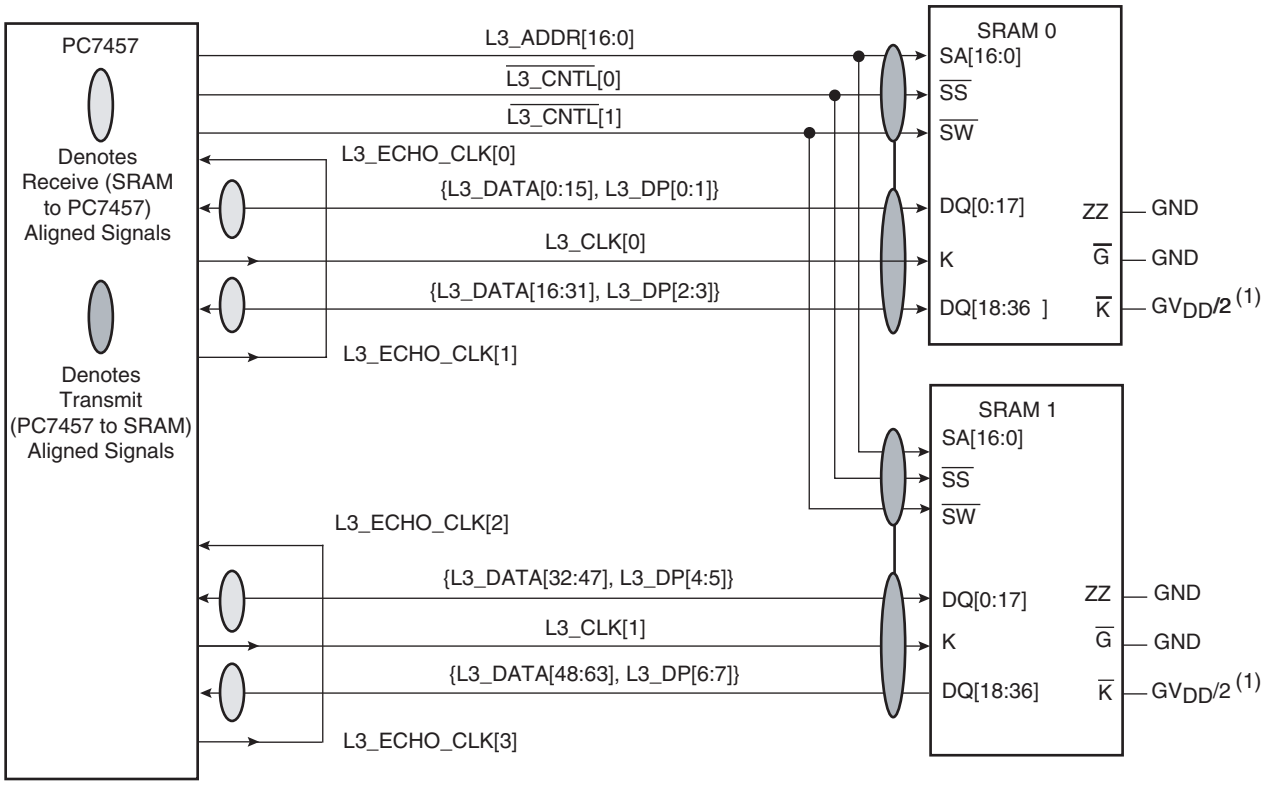
Table 7-8. L3 Bus Interface AC Timing Specifications for PB2 and Late Write SRAMs at Recommended Operating Conditions (see page 12)

Symbol	Parameter	All Speed Grades		Unit
		Min	Max	
t_{L3CR}, t_{L3CF}	L3_CLK rise and fall time(1)(2)	–	0.75	ns
t_{L3DVEH}	Setup times: Data and parity(2)(3)	0.1	–	ns
t_{L3DXEH}	Input hold times: Data and parity(2)(3)	–	0.7	ns
t_{L3CHDV}	Valid times: Data and parity(2)(4)(5)	–	2.5	ns
t_{L3CHOV}	Valid times: All other outputs(5)	–	1.8	ns
t_{L3CHDX}	Output hold times: Data and parity(2)(4)(5)	1.4	–	ns
t_{L3CHOX}	Output hold times: All other outputs(2)(5)	1.0	–	ns
t_{L3CHDZ}	L3_CLK to high impedance: Data and parity(2)	–	3.0	ns
t_{L3CHOZ}	L3_CLK to high impedance: All other outputs(2)	–	3.0	ns

Notes: 1. Rise and fall times for the L3_CLK output are measured from 20% to 80% of GV_{DD}.
2. Timing behavior and characterization are currently being evaluated.
3. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L3_ECHO_CLKn (see Figure 7-7 on page 30). Input timings are measured at the pins.
4. All output specifications are measured from the midpoint voltage of the rising edge of L3_CLKn to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (see Figure 7-7).
5. Assumes default value of L3OHCR. See "Effects of L3OHCR Settings on L3 Bus AC Specifications" on page 27" for more information.

Figure 7-8 shows the typical connection diagram for the PC7457 interfaced to PB2 SRAMs or Late Write SRAMs.

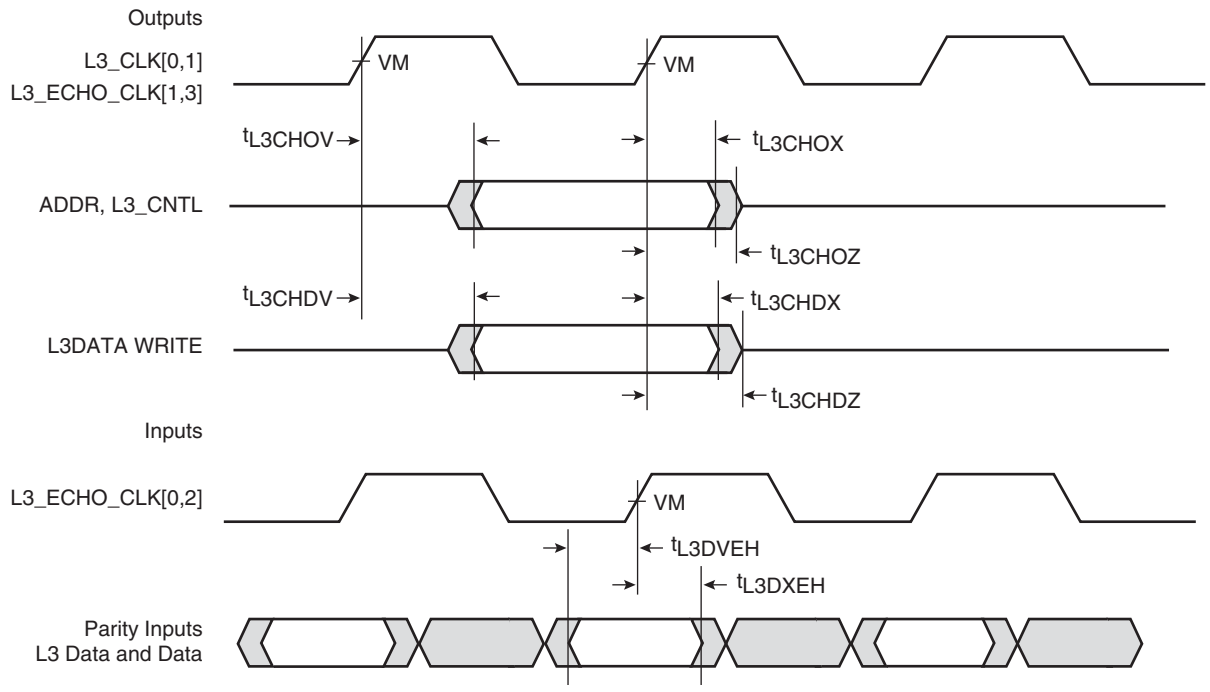
Figure 7-8. Typical Synchronous 1M Byte L3 Cache Late Write or PB2 Interface



Note: 1. Or as recommended by SRAM manufacturer for single-ended clocking.

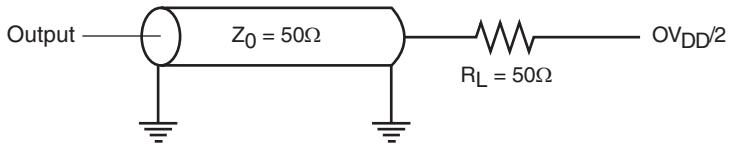
Figure 7-9 shows the L3 bus timing diagrams for the PC7457 interfaced to PB2 or Late Write SRAMs.

Figure 7-9. L3 Bus Timing Diagrams for Late Write or PB2 SRAMs



Note: VM = Midpoint Voltage ($GV_{DD}/2$)

Figure 7-10. AC Test Load



7.2.6 IEEE 1149.1 AC Timing Specifications

Table 7-9 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 7-12 through Figure 7-15 on page 35.

Table 7-9. JTAG AC Timing Specifications (Independent of SYSCLK)()at Recommended Operating Conditions (see "Recommended Operating Conditions(1)" on page 12)

Symbol	Parameter	Min	Max	Unit
f_{TCLK}	TCK frequency of operation	0	33.3	MHz
t_{TCLK}	TCK cycle time	30	–	ns
t_{JHJL}	TCK clock pulse width measured at 1.4V	15	–	ns
t_{JR} and t_{JF}	TCK rise and fall times	0	2	ns
t_{TRST}(2)	$\overline{TRST}$ assert time	25	–	ns

Table 7-9. JTAG AC Timing Specifications (Independent of SYSCLK)()at Recommended Operating Conditions (see "Recommended Operating Conditions(1)" on page 12) (Continued)

Symbol	Parameter	Min	Max	Unit
	Input Setup Times:			
t_{DVJH}(3)	Boundary-scan data	4	–	ns
t_{IVJH}	TMS, TDI	0	–	
	Input Hold Times:			
t_{DXJH}(3)	Boundary-scan data	20	–	ns
t_{IXJH}	TMS, TDI	25	–	
	Valid Times:			
t_{JLDV}(4)	Boundary-scan data	4	20	ns
t_{JLOV}	TDO	4	25	
	Output hold times:			
t_{JLDX}(4)	Boundary-scan data	TBD	TBD	
t_{JLOX}	TDO	TBD	TBD	
	TCK to output high impedance:			
t_{JLDZ}(4)(5)	Boundary-scan data	3	19	ns
t_{JLOZ}	TDO	3	9	

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (see Figure 7-11). Time-of-flight delays must be added for trace lengths, vias and connectors in the system.
2. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization

Figure 7-11 provides the AC test load for TDO and the boundary-scan outputs of the PC7457.

Figure 7-11. Alternate AC Test Load for the JTAG Interface

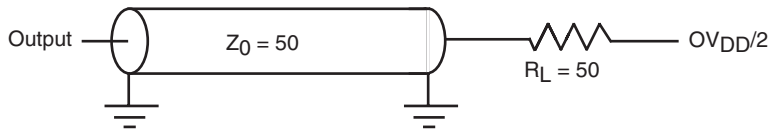
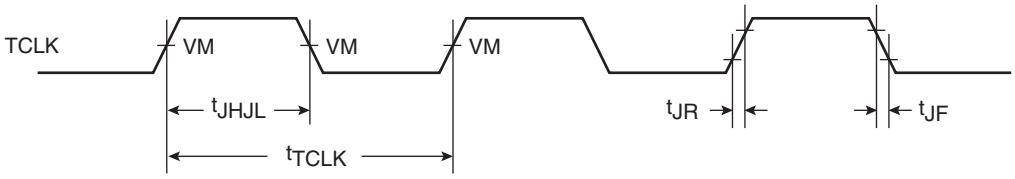
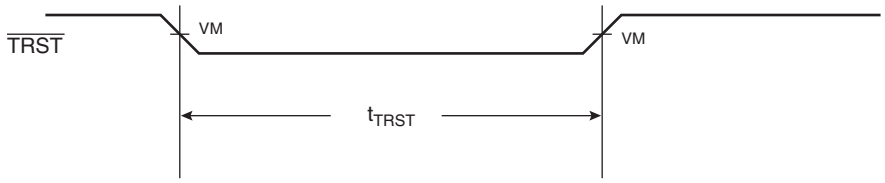


Figure 7-12. JTAG Clock Input Timing Diagram



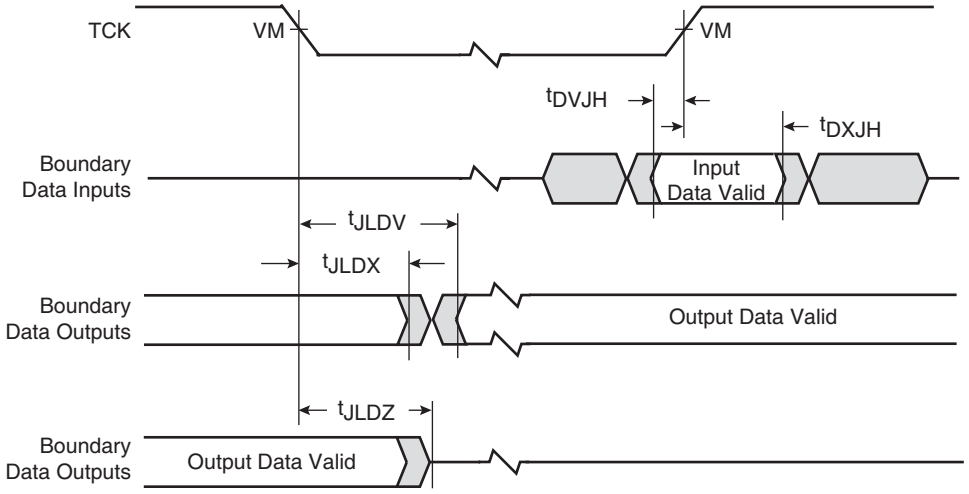
Note: VM = Midpoint Voltage (OV_{DD}/2)

Figure 7-13. $\overline{\text{TRST}}$ Timing Diagram



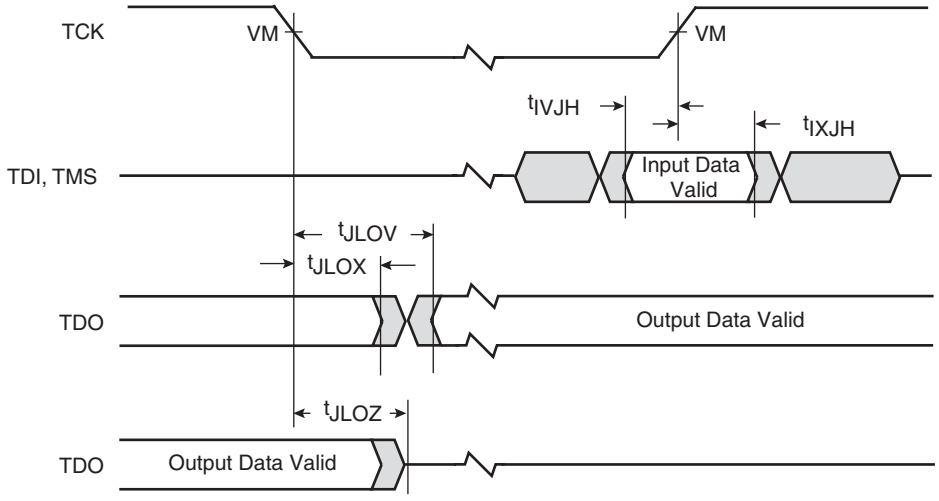
Note: VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 7-14. Boundary-scan Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 7-15. Test Access Port Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

8. Preparation for Delivery

8.1 Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of static buildup. However, the following handling practices are recommended:

- Devices should be handled on benches with conductive and grounded surfaces
- Ground test equipment, tools and operator
- Do not handle devices by the leads
- Store devices in conductive foam or carriers
- Avoid use of plastic, rubber or silk in MOS areas
- Maintain relative humidity above 50% if practical

8.2 Package Parameters for the PC7457, 483 CBGA and 483 HCTE

The package parameters are as provided in the following list. The package type is 29 × 29 mm, 483-lead ceramic ball grid array (CBGA and HCTE).

Package outline	29 mm × 29 mm
Interconnects	483 (22 × 22 ball array - 1)
Pitch	1.27 mm (50 mil)
Minimum module height	–
Maximum module height	3.22 mm
Ball diameter	0.89 mm (35 mil)
Coefficient of thermal expansion	6.8 ppm/° C (CBGA) 12.3 ppm/° C (HCTE - CBGA)

Figure 8-1 shows the pinout of the PC7457, 483 CBGA and HCTE packages as viewed from the top surface.

Figure 8-2 shows the side profile of the CBGA and HCTE packages to indicate the direction of the top surface view.

Figure 8-1. Pinout of the PC7457, 483 CBGA and HCTE Package as Viewed from the Top Surface

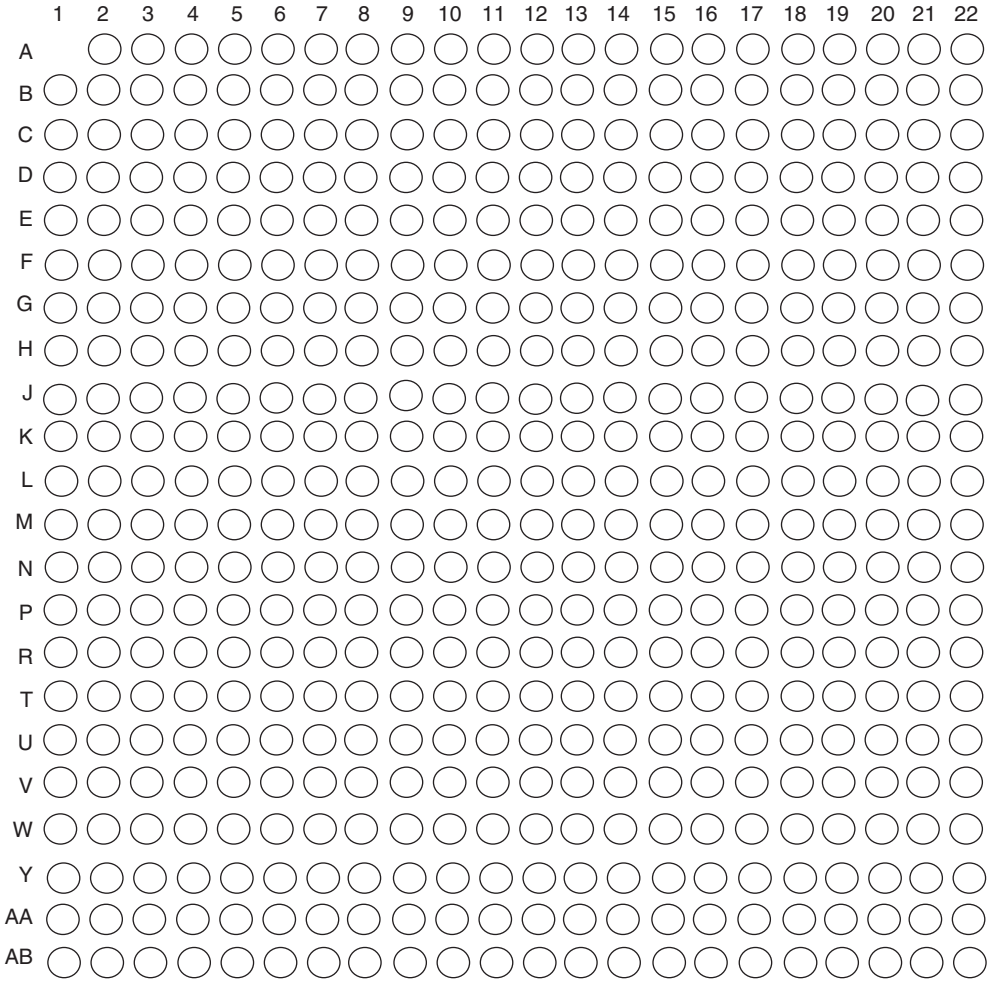


Figure 8-2. Side View of the CBGA and HCTE Packages

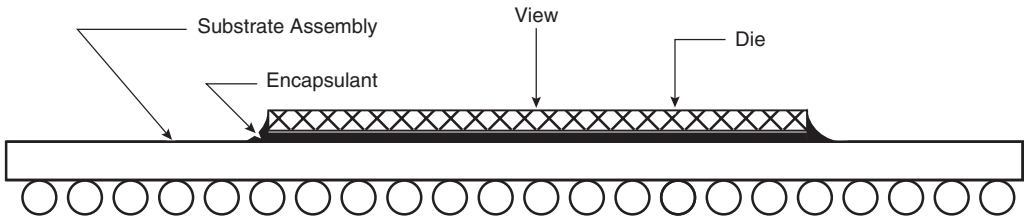


Table 8-1. Pinout Listing for the PC7457, 483 CBGA and HCTE Packages

Signal Name	Pin Number	Active	I/O	I/F Select[1]
A[0:35][2]	E10, N4, E8, N5, C8, R2, A7, M2, A6, M1, A10, U2, N2, P8, M8, W4, N6, U6, R5, Y4, P1, P4, R6, M7, N7, AA3, U4, W2, W1, W3, V4, AA1, D10, J4, G10, D9	High	I/O	BVSEL
$\overline{\text{AACK}}$	U1	Low	Input	BVSEL
AP[0:4]	L5, L6, J1, H2, G5	High	I/O	BVSEL
$\overline{\text{ARTRY}}$[3]	T2	Low	I/O	BVSEL
AVDD	B2	–	Input	N/A
$\overline{\text{BG}}$	R3	Low	Input	BVSEL
$\overline{\text{BMODE0}}$[4]	C6	Low	Input	BVSEL
$\overline{\text{BMODE1}}$[5]	C4	Low	Input	BVSEL
$\overline{\text{BR}}$	K1	Low	Output	BVSEL
BVSEL[6][7]	G6	High	Input	N/A
$\overline{\text{CI}}$[3]	R1	Low	Output	BVSEL
$\overline{\text{CKSTP\_IN}}$	F3	Low	Input	BVSEL
$\overline{\text{CKSTP\_OUT}}$	K6	Low	Output	BVSEL
CLK_OUT	N1	High	Output	BVSEL
D[0:63]	AB15, T14, R14, AB13, V14, U14, AB14, W16, AA11, Y11, U12, W13, Y14, U13, T12, W12, AB12, R12, AA13, AB11, Y12, V11, T11, R11, W10, T10, W11, V10, R10, U10, AA10, U9, V7, T8, AB4, Y6, AB7, AA6, Y8, AA7, W8, AB10, AA16, AB16, AB17, Y18, AB18, Y16, AA18, W14, R13, W15, AA14, V16, W6, AA12, V6, AB9, AB6, R7, R9, AA9, AB8, W9	High	I/O	BVSEL
$\overline{\text{DBG}}$	V1	Low	Input	BVSEL
DP[0:7]	AA2, AB3, AB2, AA8, R8, W5, U8, AB5	High	I/O	BVSEL
$\overline{\text{DRDY}}$[8]	T6	Low	Output	BVSEL
DTI[0:3])[9]	P2, T5, U3, P6	High	Input	BVSEL
EXT_QUAL[10]	B9	High	Input	BVSEL
GBL	M4	Low	I/O	BVSEL
GND	A22, B1, B5, B12, B14, B16, B18, B20, C3, C9, C21, D7, D13, D15, D17, D19, E2, E5, E21, F10, F12, F14, F16, F19, G4, G7, G17, G21, H13, H15, H19, H5, J3, J10, J12, J14, J17, J21, K5, K9, K11, K13, K15, K19, L10, L12, L14, L17, L21, M3, M6, M9, M11, M13, M19, N10, N12, N14, N17, N21, P3, P9, P11, P13, P15, P19, R17, R21, T13, T15, T19, T4, T7, T9, U17, U21, V2, V5, V8, V12, V15, V19, W7, W17, W21, Y3, Y9, Y13, Y15, Y20, AA5, AA17, AB1, AB22	–	–	N/A
GV_{DD}[11]	B13, B15, B17, B19, B21, D12, D14, D16, D18, D21, E19, F13, F15, F17, F21, G19, H12, H14, H17, H21, J19, K17, K21, L19, M17, M21, N19, P17, P21, R15, R19, T17, T21, U19, V17, V21, W19, Y21	–	–	N/A
$\overline{\text{HIT}}$[8]	K2	Low	Output	BVSEL
$\overline{\text{HRESET}}$	A3	Low	Input	BVSEL

Table 8-1. Pinout Listing for the PC7457, 483 CBGA and HCTE Packages (Continued)

Signal Name	Pin Number	Active	I/O	I/F Select[1]
$\overline{\text{INT}}$	J6	Low	Input	BVSEL
L1_TSTCLK[10]	H4	High	Input	BVSEL
L2_TSTCLK[12]	J2	High	Input	BVSEL
L3VSEL[6][7]	A4	High	Input	N/A
L3ADDR[18:0]	H11, F20, J16, E22, H18, G20, F22, G22, H20, K16, J18, H22, J20, J22, K18, K20, L16, K22, L18	High	Output	L3VSEL
L3_CLK[0:1]	V22, C17	High	Output	L3VSEL
$\overline{\text{L3\_CNTL}}$[0:1]	L20, L22	Low	Output	L3VSEL
L3DATA[0:63]	AA19, AB20, U16, W18, AA20, AB21, AA21, T16, W20, U18, Y22, R16, V20, W22, T18, U20, N18, N20, N16, N22, M16, M18, M20, M22, R18, T20, U22, T22, R20, P18, R22, M15, G18, D22, E20, H16, C22, F18, D20, B22, G16, A21, G15, E17, A20, C19, C18, A19, A18, G14, E15, C16, A17, A16, C15, G13, C14, A14, E13, C13, G12, A13, E12, C12	High	I/O	L3VSEL
L3DP[0:7]	AB19, AA22, P22, P16, C20, E16, A15, A12	High	I/O	L3VSEL
L3_ECHO_CLK[0,2]	V18, E18	High	Input	L3VSEL
L3_ECHO_CLK[1,3]	P20, E14	High	I/O	L3VSEL
$\overline{\text{LSSD\_MODE}}$[7][13]	F6	Low	Input	BVSEL
$\overline{\text{MCP}}$	B8	Low	Input	BVSEL
No Connect[14]	A8, A11, B6, B11, C11, D11, D3, D5, E11, E7, F2, F11, G2, H9	–	–	N/A
OV_{DD}	B3, C5, C7, C10, D2, E3, E9, F5, G3, G9, H7, J5, K3, L7, M5, N3, P7, R4, T3, U5, U7, U11, U15, V3, V9, V13, Y2, Y5, Y7, Y10, Y17, Y19, AA4, AA15	–	–	N/A
PLL_CFG[0:4]	A2, F7, C2, D4, H8	High	Input	BVSEL
$\overline{\text{PMON\_IN}}$[15]	E6	Low	Input	BVSEL
$\overline{\text{PMON\_OUT}}$	B4	Low	Output	BVSEL
$\overline{\text{QACK}}$	K7	Low	Input	BVSEL
$\overline{\text{QREQ}}$	Y1	Low	Output	BVSEL
$\overline{\text{SHD}}$[0:1]	L4, L8	Low	I/O	BVSEL
$\overline{\text{SMI}}$	G8	Low	Input	BVSEL
$\overline{\text{SRESET}}$	G1	Low	Input	BVSEL
SYSCLK	D6	–	Input	BVSEL
$\overline{\text{TA}}$	N8	Low	Input	BVSEL
TBEN	L3	High	Input	BVSEL
$\overline{\text{TBST}}$	B7	Low	Output	BVSEL
TCK	J7	High	Input	BVSEL
TDI[7]	E4	High	Input	BVSEL
TDO	H1	High	Output	BVSEL
$\overline{\text{TEA}}$	T1	Low	Input	BVSEL

Table 8-1. Pinout Listing for the PC7457, 483 CBGA and HCTE Packages (Continued)

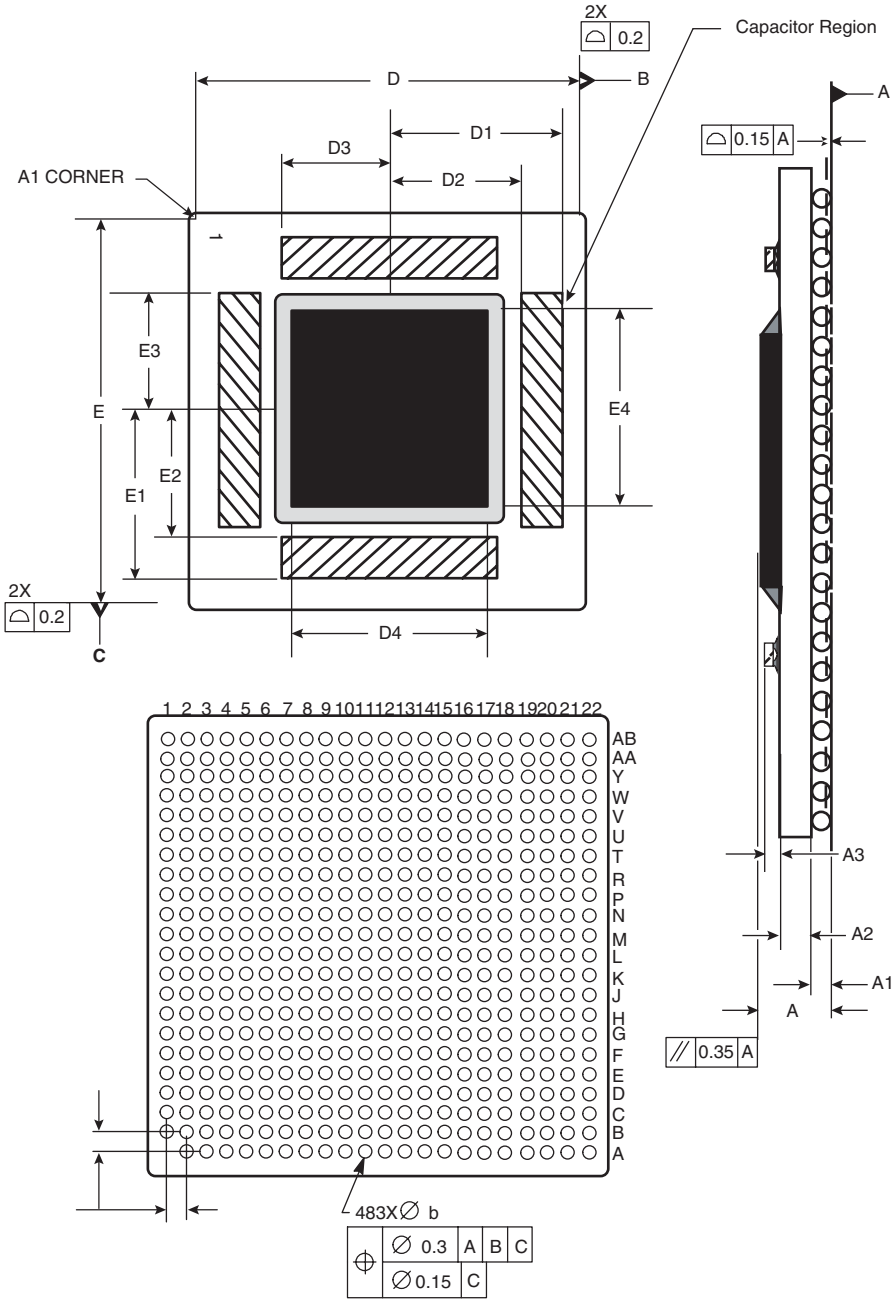
Signal Name	Pin Number	Active	I/O	I/F Select[1]
TEST[0:5][13]	B10, H6, H10, D8, F9, F8	–	Input	BVSEL
TEST[6][10]	A9	–	Input	BVSEL
TMS[7]	K4	High	Input	BVSEL
$\overline{\text{TRST}}$[7][16]	C1	Low	Input	BVSEL
$\overline{\text{TS}}$[3]	P5	Low	I/O	BVSEL
TSIZ[0:2]	L1,H3,D1	High	Output	BVSEL
TT[0:4]	F1, F4, K8, A5, E1	High	I/O	BVSEL
$\overline{\text{WT}}$[3]	L2	Low	Output	BVSEL
V_{DD}	J9, J11, J13, J15, K10, K12, K14, L9, L11, L13, L15, M10, M12, M14, N9, N11, N13, N15, P10, P12, P14	–	–	N/A
VDD_SENSE[0:1][17]	G11, J8	–	–	N/A

Notes:
1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L3 cache controls (L3CTL[0:1]); GV_{DD} supplies power to the L3 cache interface (L3ADDR[0:17], L3DATA[0:63], L3DP[0:7], L3_ECHO_CLK[0:3], and L3_CLK[0:1]) and the L3 control signals $\overline{\text{L3\_CNTL}}$[0:1]; and V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). For actual recommended value of V_{IN} or supply voltages, see "Recommended Operating Conditions[1]" on page 12.
2. Unused address pins must be pulled down to GND.
3. These pins require weak pull-up resistors (for example, 4.7 kΩ) to maintain the control signals in the negated state after they have been actively negated and released by the PC7457 and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{\text{HRESET}}$ going high.
5. This signal must be negated during reset, by pull up to OV_{DD} or negation by ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), to ensure proper operation.
6. See Table 6-1 on page 13 for bus voltage configuration information. If used, pull-down resistors should be less than 250Ω.
7. Internal pull up on die.
8. Ignored in 60x bus mode.
9. These signals must be pulled down to GND if unused or if the PC7457 is in 60x bus mode.
10. These input signals for factory use only and must be pulled down to GND for normal machine operation.
11. Power must be supplied to GV_{DD}, even when the L3 interface is disabled or unused.
12. It is recommended that this test signal be tied to $\overline{\text{HRESET}}$; however, other configurations will not adversely affect performance.
13. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
14. These signals are for factory use only and must be left unconnected for normal machine operation.
15. This pin can externally cause a performance monitor event. Counting of the event is enabled via software.
16. This signal must be asserted during reset, by pull down to GND or assertion by $\overline{\text{HRESET}}$, to ensure proper operation.
17. These pins are internally connected to V_{DD}. They are intended to allow an external device to detect the core voltage level present at the processor core. If unused, they must be connected directly to V_{DD} or left unconnected.

9. Mechanical Dimensions for the PC7457, 483 CBGA

Figure 9-1 provides the mechanical dimensions and bottom surface nomenclature for the PC7457, 483 CBGA package.

Figure 9-1. Mechanical Dimensions and Bottom Surface Nomenclature for the PC7457, 483 CBGA Package



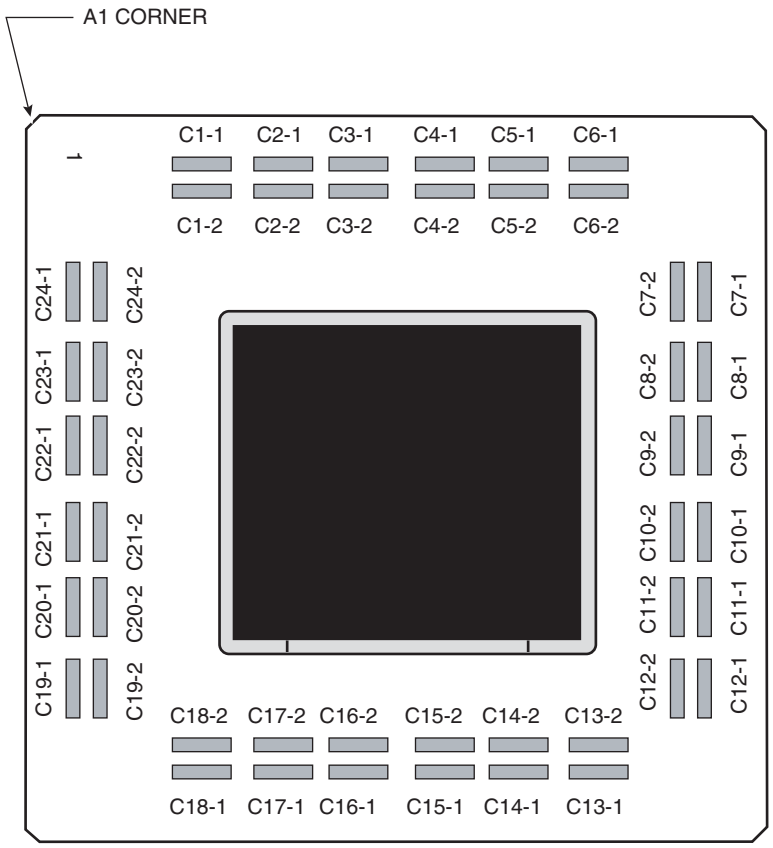
	Millimeters	
DIM	MIN	MAX
A	2.72	3.20
A1	0.80	1
A2	1.10	1.30
A3	–	0.6
b	0.82	0.93
D	29 BSC	
D1	–	12.5
D2	8.5	–
D3	–	8.4
D4	10.9	11.1
e	1.27 BSC	
E	29 BSC	
E1	–	12.5
E2	8.5	–
E3	–	8.4
E4	9.55	9.75

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metallized feature with various shapes. Bottom side. A1 corner is designated with a ball missing from the array

10. Substrate Capacitors for the PC7457, 483 CBGA

Figure 10-1 shows the connectivity of the substrate capacitor pads for the PC7457, 483 CBGA. All capacitors are 100 nF.

Figure 10-1. Substrate Bypass Capacitors for the PC7457, 483 CBGA

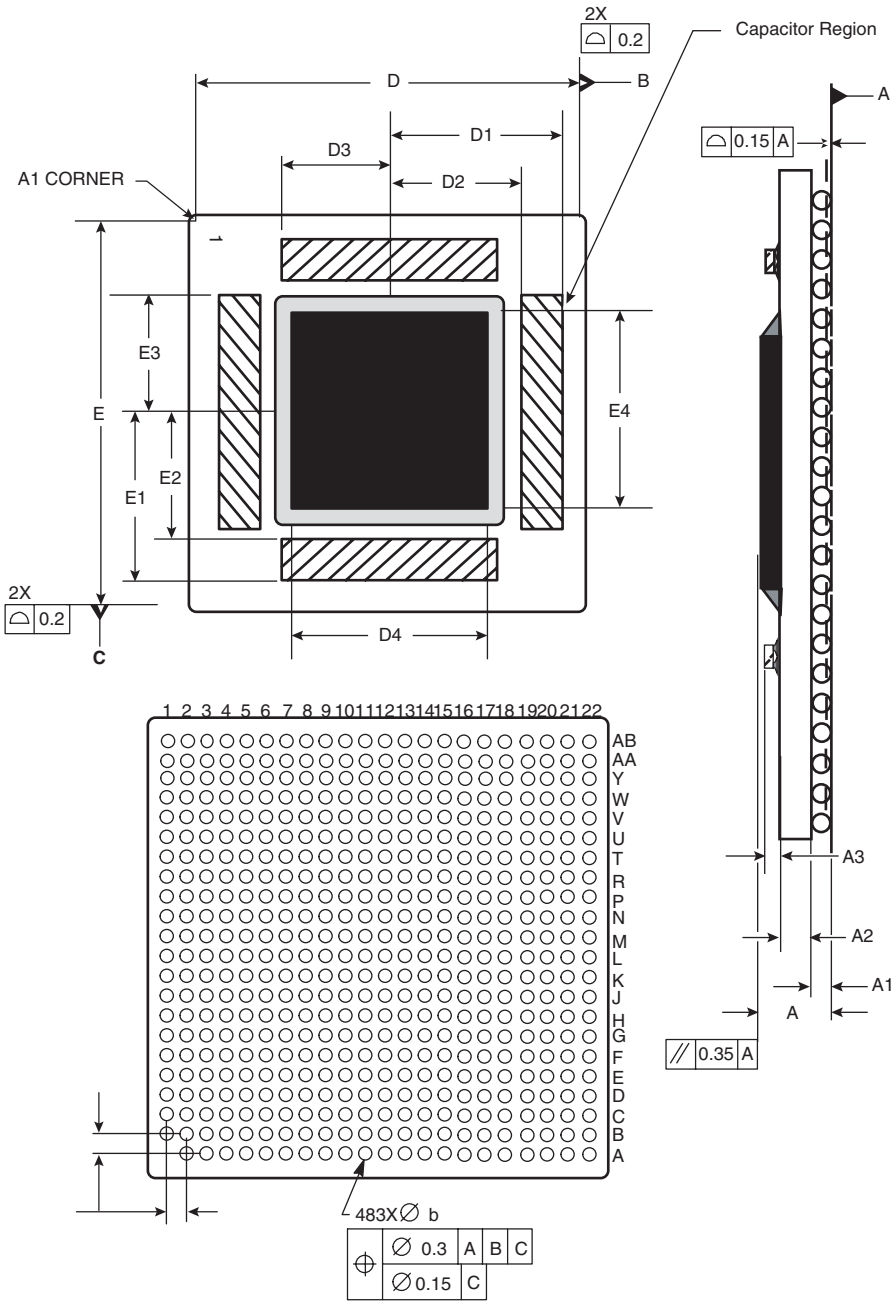


Capacitor	Pad Number	
	-1	-2
C1	GND	OV_{DD}
C2	GND	V_{DD}
C3	GND	GV_{DD}
C4	GND	V_{DD}
C5	GND	V_{DD}
C6	GND	GV_{DD}
C7	GND	V_{DD}
C8	GND	V_{DD}
C9	GND	GV_{DD}
C10	GND	V_{DD}
C11	GND	V_{DD}
C12	GND	GV_{DD}
C13	GND	V_{DD}
C14	GND	V_{DD}
C15	GND	V_{DD}
C16	GND	OV_{DD}
C17	GND	V_{DD}
C18	GND	OV_{DD}
C19	GND	V_{DD}
C20	GND	V_{DD}
C21	GND	OV_{DD}
C22	GND	V_{DD}
C23	GND	V_{DD}
C24	GND	V_{DD}

11. Mechanical Dimensions for the PC7457, 483 HCTE

Figure 11-1 provides the mechanical dimensions and bottom surface nomenclature for the PC7457, 483 HCTE package.

Figure 11-1. Mechanical Dimensions and Bottom Surface Nomenclature for the PC7457, 483 HCTE Package



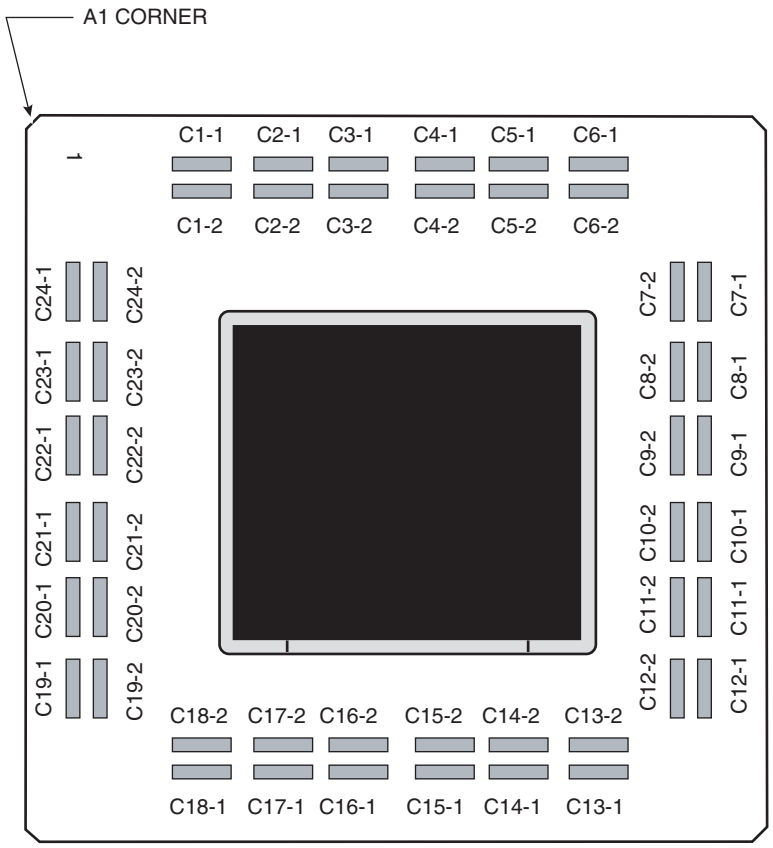
	Millimeters	
DIM	MIN	MAX
A	2.72	3.20
A1	0.80	1
A2	1.10	1.30
A3	–	0.6
b	0.82	0.93
D	29 BSC	
D1	–	12.5
D2	8.5	–
D3	–	8.4
D4	10.9	11.1
e	1.27 BSC	
E	29 BSC	
E1	–	12.5
E2	8.5	–
E3	–	8.4
E4	9.55	9.75

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metallized feature with various shapes. Bottom side. A1 corner is designated with a ball missing from the array

12. Substrate Capacitors for the PC7457, 483 HCTE

Figure 12-1 shows the connectivity of the substrate capacitor pads for the PC7457, 483 HCTE. All capacitors are 100 nF.

Figure 12-1. Substrate Bypass Capacitors for the PC7457, 483 HCTE

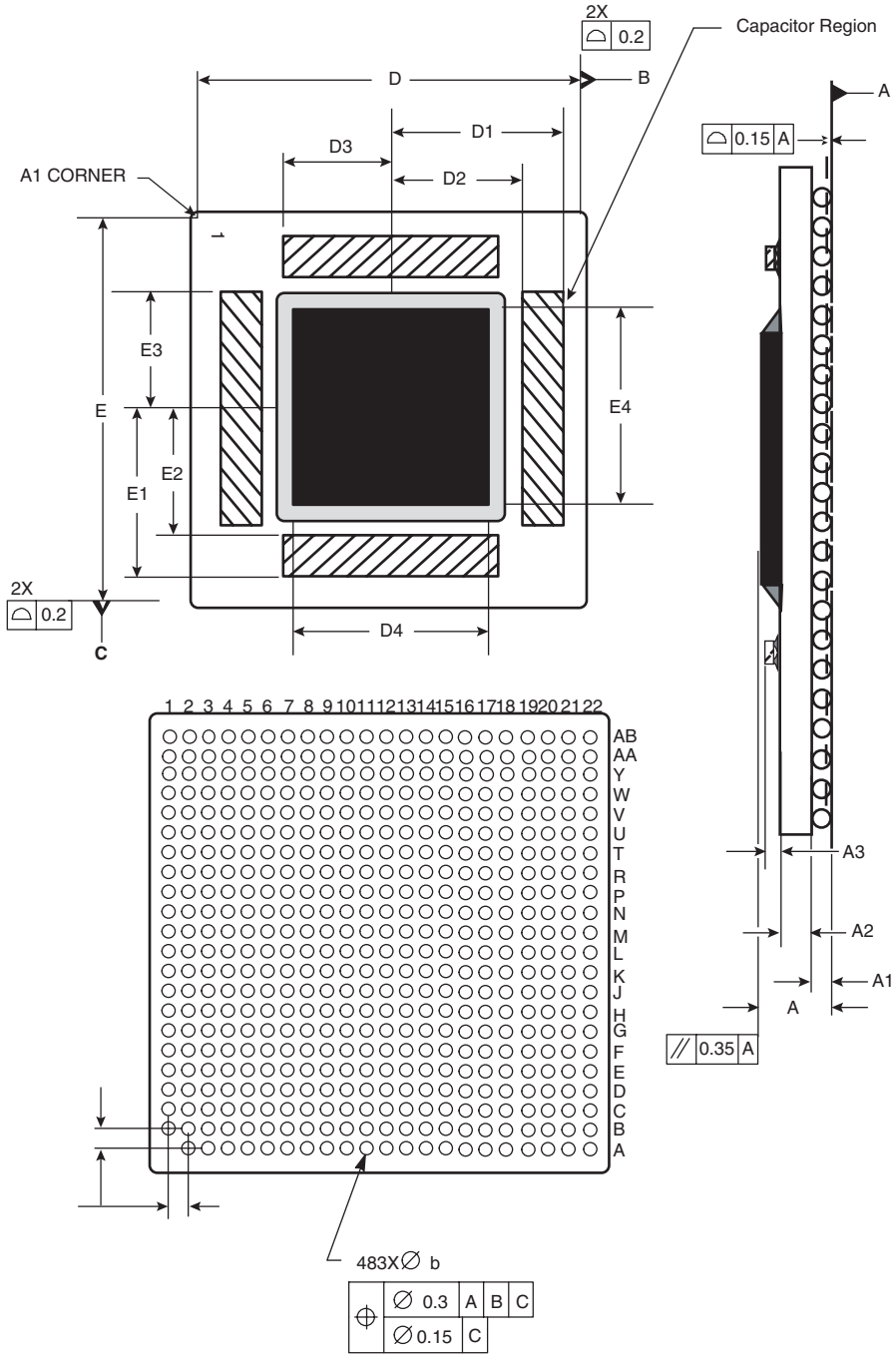


Capacitor	Pad Number	
	-1	-2
C1	GND	OV_{DD}
C2	GND	V_{DD}
C3	GND	GV_{DD}
C4	GND	V_{DD}
C5	GND	V_{DD}
C6	GND	GV_{DD}
C7	GND	V_{DD}
C8	GND	V_{DD}
C9	GND	GV_{DD}
C10	GND	V_{DD}
C11	GND	V_{DD}
C12	GND	GV_{DD}
C13	GND	V_{DD}
C14	GND	V_{DD}
C15	GND	V_{DD}
C16	GND	OV_{DD}
C17	GND	V_{DD}
C18	GND	OV_{DD}
C19	GND	V_{DD}
C20	GND	V_{DD}
C21	GND	OV_{DD}
C22	GND	V_{DD}
C23	GND	V_{DD}
C24	GND	V_{DD}

13. Mechanical Dimensions for the PC7457, 483 HCTE ROHS compliant

Figure 13-1 provides the mechanical dimensions and bottom surface nomenclature for the PC7457, 483 HCTE package.

Figure 13-1. Mechanical Dimensions and Bottom Surface Nomenclature for the PC7457, 483 HCTE Package

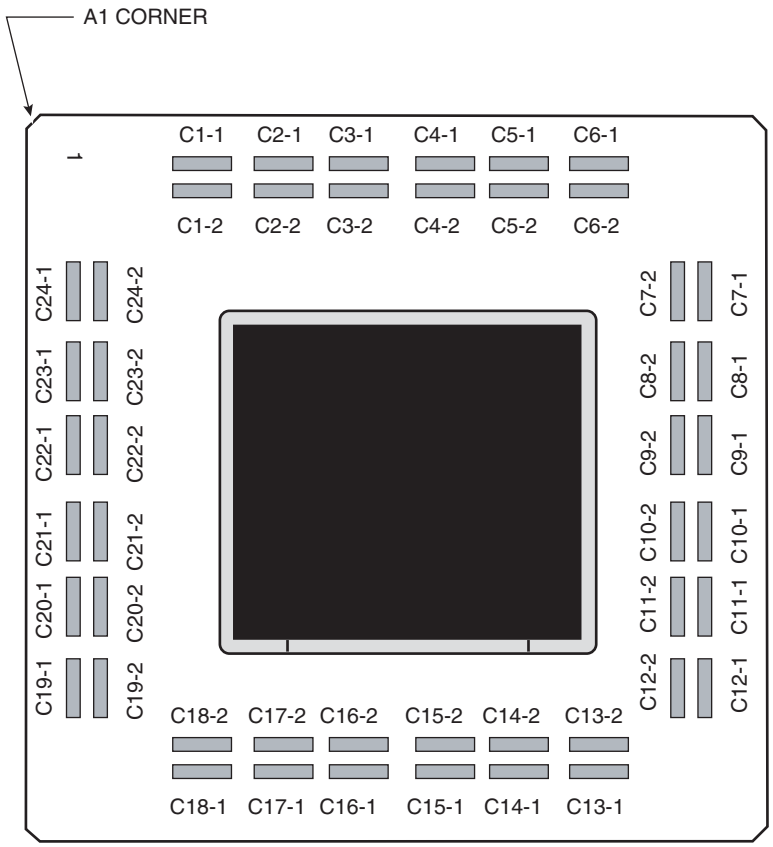


	Millimeters	
DIM	MIN	MAX
A	2.32	2.80
A1	0.4	0.6
A2	1.10	1.30
A3	–	0.6
b	0.6	0.9
D	29 BSC	
D1	–	12.5
D2	8.5	–
D3	–	8.4
D4	10.9	11.1
e	1.27 BSC	
E	29 BSC	
E1	–	12.5
E2	8.5	–
E3	–	8.4
E4	9.55	9.75

14. Substrate Capacitors for the PC7457, 483 HCTE ROHS Compliant

Figure 12-1 shows the connectivity of the substrate capacitor pads for the PC7457, 483 HCTE. All capacitors are 100 nF.

Figure 14-1. Substrate Bypass Capacitors for the PC7457, 483 HCTE



Capacitor	Pad Number	
	-1	-2
C1	GND	OV_{DD}
C2	GND	V_{DD}
C3	GND	GV_{DD}
C4	GND	V_{DD}
C5	GND	V_{DD}
C6	GND	GV_{DD}
C7	GND	V_{DD}
C8	GND	V_{DD}
C9	GND	GV_{DD}
C10	GND	V_{DD}
C11	GND	V_{DD}
C12	GND	GV_{DD}
C13	GND	V_{DD}
C14	GND	V_{DD}
C15	GND	V_{DD}
C16	GND	OV_{DD}
C17	GND	V_{DD}
C18	GND	OV_{DD}
C19	GND	V_{DD}
C20	GND	V_{DD}
C21	GND	OV_{DD}
C22	GND	V_{DD}
C23	GND	V_{DD}
C24	GND	V_{DD}

15. System Design Information

This section provides system and thermal design recommendations for successful application of the PC7457.

15.1 Clocks

The following sections provide more detailed information regarding the clocking o fthe PC7457.

15.1.1 Core Clocks and PLL Configuration

The PC7457 PLL is configured by the PLL_CFG[0:4] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the PC7457 is shown in Table 15-1 for a set of example frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the 1-GHz column in Table 7-2 on page 20. Note that these configurations were different in some earlier PC7450-family devices and care should be taken when upgrading to the PC7457 to verify the correct PLL settings for an application.

Table 15-1. PC7457 Microprocessor PLL Configuration Example for 1267 MHz Parts

			Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
			Bus (SYSCLK) Frequency							
PLL_CFG[0:4]	Bus-to-Core Multiplier	Core-to-VCO Multiplier	33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz
01000	2x	2x								
10000	3x	2x								
10100	4x	2x								667 (1333)
10110	5x	2x							667 (1333)	835 (1670)
10010	5.5x	2x							733 (1466)	919 (1837)
11010	6x	2x						600 (1200)	800 (1600)	1002 (2004)
01010	6.5x	2x						650 (1300)	866 (1730)	1086 (2171)
00100	7x	2x						700 (1400)	931 (1862)	1169 (2338)
00010	7.5x	2x					623 (1245)	750 (1500)	1000 (2000)	1253 (2505)
11000	8x	2x				600 (1200)	664 (1328)	800 (1600)	1064 (2128)	
01100	8.5x	2x				638 (1276)	706 (1412)	850 (1700)	1131 (2261)	
01111	9x	2x			600 (1200)	675 (1350)	747 (1494)	900 (1800)	1197 (2394)	
01110	9.5x	2x			633 (1266)	712 (1524)	789 (1578)	950 (1900)	1264 (2528)	

Table 15-1. PC7457 Microprocessor PLL Configuration Example for 1267 MHz Parts (Continued)

PLL_CFG[0:4]	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
			Bus (SYSCLK) Frequency							
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz
10101	10x	2x			667 (1333)	750 (1500)	830 (1660)	1000 (2000)		
10001	10.5x	2x			700 (1400)	938 (1876)	872 (1744)	1050 (2100)		
10011	11x	2x			733 (1466)	825 (1650)	913 (1826)	1100 (2200)		
00000	11.5x	2x			766 (532)	863 (1726)	955 (1910)	1150 (2300)		
10111	12x	2x		600 (1200)	800 (1600)	900 (1800)	996 (1992)	1200 (2400)		
11111	12.5x	2x		600 (1200)	833 (1666)	938 (1876)	1038 (2076)	1250 (2500)		
01011	13x	2x		650 (1300)	865 (1730)	975 (1950)	1079 (2158)			
11100	13.5x	2x		675 (1350)	900 (1800)	1013 (2026)	1121 (2242)			
11001	14x	2x		700 (1400)	933 (1866)	1050 (2100)	1162 (2324)			
00011	15x	2x		750 (1500)	1000 (2000)	1125 (2250)	1245 (2490)			
11011	16x	2x		800 (1600)	1066 (2132)	1200 (2400)				
00001	17x	2x		850 (1900)	1132 (2264)					
00101	18x	2x	600 (1200)	900 (1800)	1200 (2400)					
00111	20x	2x	667 (1334)	1000 (2000)						
01001	21x	2x	700 (1400)	1050 (2100)						
01101	24x	2x	800 (1600)	1200 (2400)						
11101	28x	2x	933 (1866)							
00110	PLL bypass		PLL off, SYSCLK clocks core circuitry directly							
11110	PLL off		PLL off, no core clocking occurs							

Notes: 1. PLL_CFG[0:4] settings not listed are reserved.

2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the PC7455; See “Clock AC Specifications” on page 20. for valid SYSCLK, core, and VCO frequencies.

3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly and the PLL is disabled. However, the bus interface unit requires a 2x clock to function. Therefore, an additional signal, EXT_QUAL, must be driven at one-half the frequency of SYSCLK and offset in phase to meet the required input setup t_{IVKH} and hold time t_{IXKH} (see Table 7-3 on page 22). The result is that the processor bus frequency is one-half SYSCLK while the internal processor is clocked at SYSCLK frequency. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the PC7455 regardless of the SYSCLK input.

15.1.2 L3 Clocks

The PC7457 generates the clock for the external L3 synchronous data SRAMs by dividing the core clock frequency of the PC7457. The core-to-L3 frequency divisor for the L3 PLL is selected through the L3_CLK bits of the L3CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the PC7457 core, and timing analysis of the circuit board routing. Table 15-2 shows various example L3 clock frequencies that can be obtained for a given set of core frequencies.

Table 15-2. Sample Core-to-L3 Frequencies[1]

Core Frequency (MHz)	÷2	÷2.5	÷3	÷3.5	÷4	÷4.5	÷5	÷5.5	÷6	÷6.5	÷7	÷7.5	÷8
500	250	200	167	143	125	111	100	91	83	77	71	67	63
533	266	213	178	152	133	118	107	97	89	82	76	71	67
550	275	220	183	157	138	122	110	100	92	85	79	73	69
600	300	240	200	171	150	133	120	109	100	92	86	80	75
650	325	260	217	186	163	144	130	118	108	100	93	87	81
666	333	266	222	190	167	148	133	121	111	102	95	89	83
700	350	280	233	200	175	156	140	127	117	108	100	93	88
733	367	293	244	209	183	163	147	133	122	113	105	98	92
800	400	320	266	230	200	178	160	145	133	123	114	107	100
866	433	347	289	248	217	192	173	157	145	133	124	115	108
933	467	373	311	266	233	207	187	170	156	144	133	124	117
1000	500	400	333	285	250	222	200	182	166	154	143	133	125
1050[2]	525	420	350	300	263	233	191	191	175	162	150	140	131
1100[2]	550	440	367	314	275	244	200	200	183	169	157	147	138
1150[2]	575	460	383	329	288	256	209	209	192	177	164	153	144
1200[2]	600	480	400	343	300	267	218	218	200	185	171	160	150
1250[2]	638	500	417	357	313	278	227	227	208	192	179	167	156
1300[2]	650	520	433	371	325	289	236	236	217	200	186	173	163

Notes:
1. The core and L3 frequencies are for reference only. Note that maximum L3 frequency is design dependent. Some examples may represent core or L3 frequencies which are not useful, not supported, or not tested for the PC7457; see "L3 Clock AC Specifications" on page 24 for valid L3_CLK frequencies and for more information regarding the maximum L3 frequency.
2. Not all core frequencies are supported by all speed grades; see Table 7-2 on page 20 for minimum and maximum core frequency specifications.

15.1.3 System Bus Clock (SYSCLK) and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 7-2 on page 20 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the PC7457 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the PC7457 is compatible with spread spectrum sources if the recommendations listed in Table 20 are observed.

Table 15-3. Spread Specturm Clock Source Recommendations (at Recommended Operating Conditions, see page 12.)

Parameter	Min	Max	Unit	Notes
Frequency modulation	–	50	kHz	(1)
Frequency spread	–	1.0	%	(1)(2)

Notes: 1. Guaranteed by design.

2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 7-2 on page 20.

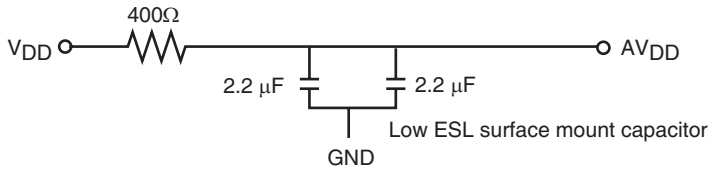
It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core or bus frequency should avoid violating the stated limits by using down-spreading only.

15.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the PC7457 to provide power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500_kHz to 10 MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 9-1 using surface mount capacitors with minimum effective series inductance (ESL) is recommended.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 CBGA footprint and very close to the periphery of the 483 CBGA footprint, without the inductance of vias.

Figure 15-1. PLL Power Supply Filter Circuit



Previous revisions of this document required a 400Ω resistor for Rev. 1.1 (Rev. B) devices instead of the 10Ω resistor shown above. All production devices require a 10Ω resistor. For more information, see the PC7450 Family Chip Errata for the PC7457 and PC7447.

15.3 Decoupling Recommendations

Due to the PC7457 dynamic power management feature, large address and data buses, and high operating frequencies, the PC7457 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PC7457 system, and the PC7457 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and GV_{DD} pin of the PC7457. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}/GV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance, preferably 0508 or 0603 orientations where connections are made along the length of the part. Consistent with the recommendations of Dr. Howard Johnson in High Speed Digital Design: A Handbook of Black Magic (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, GV_{DD}, and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors: 100 – 330 µF (AVX TPS tantalum or Sanyo OSCON).

15.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD}, OV_{DD}, GV_{DD}, and GND pins in the PC7457. If the L3 interface is not used, GV_{DD} should be connected to the OV_{DD} power plane, and L3VSEL should be connected to BVSEL; the remainder of the L3 interface may be left unterminated.

15.5 Output Buffer DC Impedance

The PC7457 processor bus and L3 I/O drivers are characterized over process, voltage, and temperature.

To measure Z0, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 10-1 on page 42).

The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and RN is trimmed until the voltage at the pad equals $OV_{DD}/2$. RN then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and RP is trimmed until the voltage at the pad equals $OV_{DD}/2$. RP then becomes the resistance of the pull-up devices. RP and RN are designed to be close to each other in value. Then, Z0 = (RP + RN)/2.

Figure 15-2. Driver Impedance Measurement

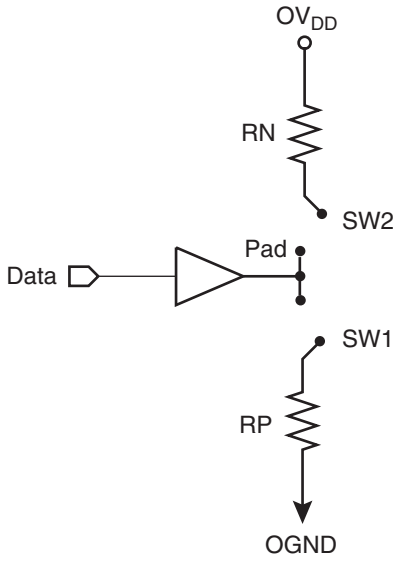


Table 15-4 summarizes the signal impedance results. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 15-4. Impedance Characteristics with V_{DD} = 1.5V, OV_{DD} = 1.8V ±5%, T_J = 5° - 85° C

Impedance		Processor bus	L3 Bus	Unit
Z_0	Typical	33 – 42	34 – 42	Ω
	Maximum	31 – 51	32 – 44	Ω

15.6 Pull-up/Pull-down Resistor Requirements

The PC7457 requires high-resistive (weak: 4.7 kΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the PC7457 or other bus masters. These pins are $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHDO}$, and $\overline{SHD1}$.

Some pins designated as being for factory test must be pulled up to OVDD or down to GND to ensure proper device operation. For the PC7447, 360 BGA, the pins that must be pulled up to OVDD are $\overline{LSSD\_MODE}$ and TEST[0:3]; the pins that must be pulled down to GND are L1_$\overline{TSTCLK}$ and TEST[4]. For the PC7457, 483 BGA, the pins that must be pulled up to OVDD are $\overline{LSSD\_MODE}$ and TEST[0:5]; the pins that must be pulled down are L1_TSTCLK and TEST[6]. The $\overline{CKSTP\_IN}$ signal should likewise be pulled up through a pull-up resistor (weak or stronger: 4.7 – 1 kΩ) to prevent erroneous assertions of this signal. In addition, the PC7457 has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7 – 1 kΩ) if it is used by the system. This pin is $\overline{CKSTP\_OUT}$.

If pull-down resistors are used to configure BVSEL or L3VSEL, the resistors should be less than 250Ω. Because PLL_CFG[0:4] must remain stable during normal operation, strong pull-up and pull-down resistors (1 kΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise or noise coupling.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Because the PC7457 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the PC7457 or by other receivers in the system. It is recommended that these signals be pulled up through weak (4.7 kΩ) pull-up resistors by the system, or that they may be otherwise driven by the system during inactive periods of the bus. The snooped address and transfer attribute inputs are A[0:35], AP[0:4], TT[0:4], $\overline{\text{CI}}$, $\overline{\text{WT}}$, and $\overline{\text{GBL}}$.

If extended addressing is not used, A[0:3] are unused and must be pulled low to GND through weak pull-down resistors. If the PC7457 is in 60x bus mode, DTI[0:3] must be pulled low to GND through weak pull-down resistors.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, don't require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are D[0:63] and DP[0:7].

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins don't require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, then all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

The L3 interface does not normally require pull-up resistors.

15.7 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 15-1 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. While Freescale recommends that the COP header be designed into the system as shown in Figure 15-1 on page 50, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

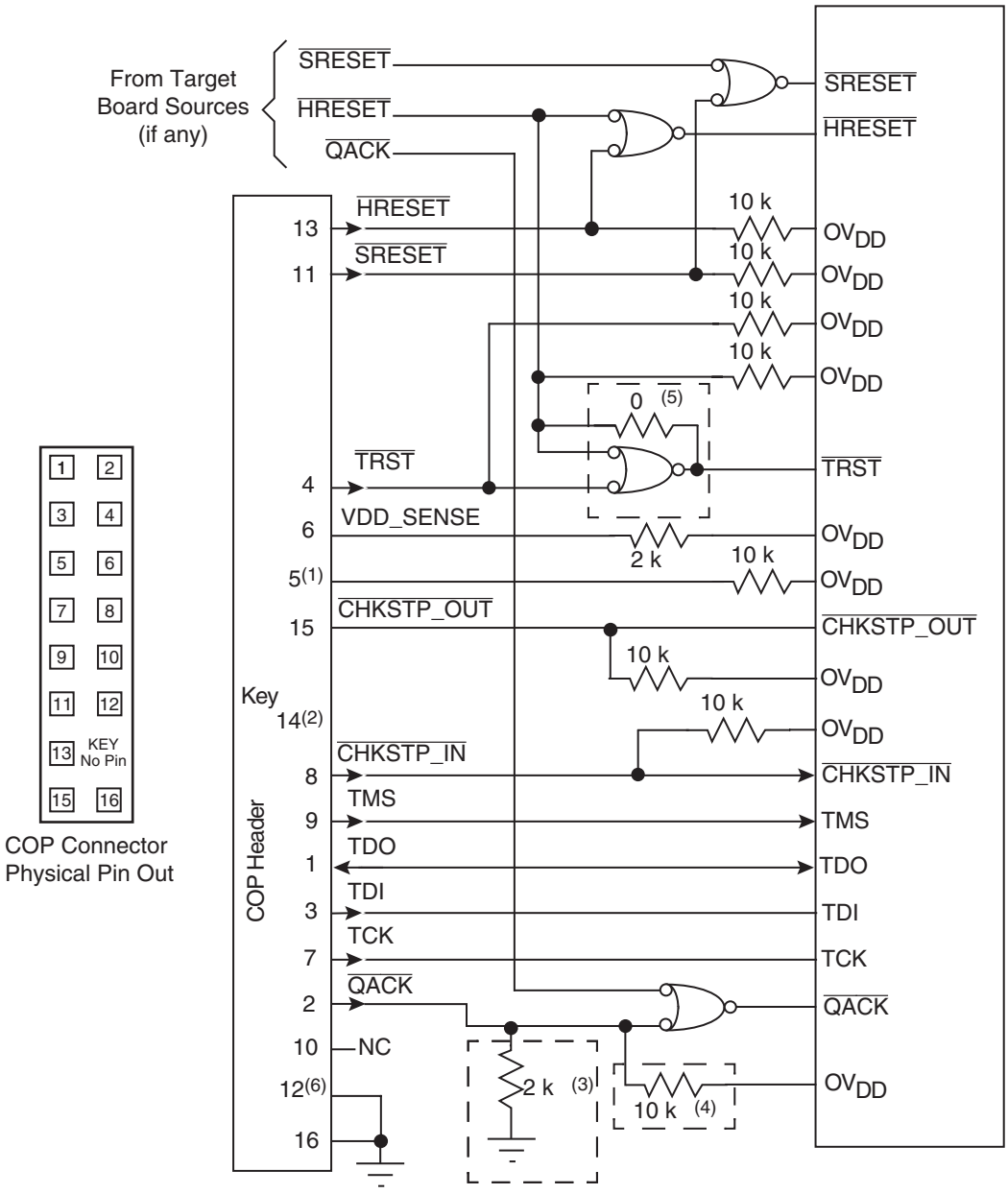
The COP header shown in Figure 15-1 adds many benefits – breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface – and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 15-1; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 15-1 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 15-1 is usually connected to the PCI bridge chip in a system and is an input to the PC7457 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the PC7457 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is deasserted when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged via logic so that it also can be driven by the PCI bridge.

Figure 15-3. JTAG Interface Connection



Notes:
1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the PC7457. Connect pin 5 of the COP header to OV_{DD} with a 10 kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively deassert $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0Ω isolation resistor.
6. Though defined as a No-Connect, it is a common and recommended practice to use pin 12 as an additional GND pin for improved signal integrity.

16. Definitions

16.1 Life Support Applications

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Atmel customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Atmel for any damages resulting from such improper use or sale.

17. Ordering Information

xx	7457	y	xxx	y	nnn	N	x
Product Code[1]	Part Identifier	Temperature Range: T_J[1]	Package[1]	Screening Level	Max Internal Processor Speed[1]	Application Modifier[1]	Revision Level[1]
PC(X)[2]	7457	M: -55˚C, +125˚C V: -40˚C, 110˚C	G: CBGA GH: HiTCE GHY: HiTCE ROHS compliant	U: Upscreening (CBGA) Blank: standard	933 MHz 1000 MHz	N: 1.1V ± 50 mV	C

Notes:
1. For availability of the different versions, contact your local Atmel sales office.
2. The letter X in the part number designates a "Prototype" product that has not been qualified by Atmel. Reliability of a PCX part-number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.

18. Document Revision History

Table 18-1 provides a revision history for this hardware specification.

Table 18-1. Document Revision History

Revision Number	Date	Substantive Change(s)
D	03/06	Remove PC7447. Modification Table 6-1 on page 13? and ordering information
C	06/2005	Updated document to new Atmel template
		Updated section numbering and changed reference from part number specifications to addendums
		Added Rev. 1.2 devices, including increased L3 clock max frequency to 250 MHz and improved L3 AC timing
		Table 6-2 on page 13: Added CTE information
		Table 7-2 on page 20: Modified jitter specifications to conform to JEDEC standards, changed jitter specification to cycle-to-cycle jitter (instead of long- and short-term jitter); changed jitter bandwidth recommendations
		Table 7-7 on page 29: Deleted note 9 and renumbered.
		Table 7-8 on page 31: Deleted note 5 and renumbered
		Table 8-1 on page 38: Revised note 6
		Added Section 15.1.3 ”System Bus Clock (SYSCLK) and Spread Spectrum Sources” on page 50
		Section 15.2 ”PLL Power Supply Filtering” on page 50: Changed filter resistor recommendations. Recommend 10Ω resistor for all production devices, including production Rev. 1.1 devices. 400Ω resistor needed only for early Rev. 1.1 devices.
		Table 18-1: Reversed the order of revision numbers.
		Section 15.1.1 on page 47: Corrected note regarding different PLL configurations for earlier devices; all PC7457 devices to date conform to this table
		Section 15.6 on page 52: Added information about unused L3_ADDR signals.
		HCTE package information
		Preliminary specification α-site release subsequent to preliminary specification β-site Motorola changed to Freescale
B	11/2004	Figure 7-3 on page 22: Corrected pin lists for input and output AC timing to correctly show $\overline{\text{HIT}}$ as an output-only signal
		Added specifications for 1267 MHz devices; removed specs for 1300 MHz devices.
		Changed recommendations regarding use of L3 clock jitter in AC timing analysis in Section “L3 Clock AC Specifications” on page 24; the L3 jitter is now fully comprehended in the AC timing specs and does not need to be included in the timing analysis

Table of Contents

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
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13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
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Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
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