High Performance Regulators for PCs

Switching Regulator for DDR-SDRAM Cores

BD9535MUV

No.10030EBT34

●Description

BD9535MUV is a 2ch switching regulator controller with high output current which can achieve low output voltage (0.7V～2.0V) from a wide input voltage range (4.5V～25V). High efficiency for the switching regulator can be realized by utilizing an external N-MOSFET power transistor. A new technology called H^{3}Reg^{TM} is a Rohm proprietary control method to realize ultra high transient response against load change. SLLM^{TM} (Simple Light Load Mode) technology is also integrated to improve efficiency in light load mode, providing high efficiency over a wide load range. For the soft start/stop function, variable frequency function, short circuit protection function with timer latch, and tracking function are all built in. This 2ch switching regulator is specially designed for Chipset and Front Side Bus.

●Features

1) 2ch H^{3}REG^{TM} Switching Regulator Controller
2) Light Load Mode and Continuous Mode Changeable
3) Thermal Shut Down (TSD), Under Voltage LockOut (UVLO),
   Over Current (detect the peak current) Protection (OCP), Over Voltage Protection (OVP),
   Short circuit protection with built-in timer-latch
4) Soft start function to minimize rush current during startup
5) Switching Frequency Variable (f=200KHz～600kHz)
6) VQFN032V5050 package
7) Built-in Power good circuit
8) Adjustable to chip set spec by tracking function

●Applications

Laptop PC, Desktop PC, LCD-TV, Digital Components

●Maximum Absolute Ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Input Voltage 1	V_{CC}	7 *1	V
Input Voltage 2	V_{DD}	7 *1	V
Input Voltage 3	V_{IN}	30 *1	V
BOOT Voltage	$V_{BOOT1/2}$	35 *1	V
BOOT-SW Voltage	V_{BOOT1}-V_{SW1}, V_{BOOT2}-V_{SW2}	7 *1	V
HG-SW Voltage	V_{HG1}-V_{SW1}, V_{HG2}-V_{SW2}	7 *1	V
LG Voltage	$V_{LG1/2}$	V_{DD}	V
Setting for Output Voltage	$V_{REF1/2}$	V_{CC}	V
Output voltage	$V_{Is+1/2}$, $V_{Is-1/2}$	V_{CC}	V
SS Voltage	$V_{SS1/2}$	V_{CC}	V
FS Voltage	V_{FS}	V_{CC}	V
VREG voltage	V_{REG}	V_{CC}	V
Current Limit setting Voltage	$V_{ILIM1/2}$	V_{CC}	V
Logic Input Voltage	$V_{EN1/2}$	7 *1	V
PGOOD Voltage	$V_{PGOOD1/2}$	7 *1	V
CE Voltage	$V_{CE1/2}$	7 *1	V
Power dissipation	Pd	T.B.D	W
Operating Temperature Range	Topr	-10～+100	℃
Storage Temperature Range	Tstg	-55～+150	℃
Junction Temperature	Tjmax	+150	℃

*1 Not to exceed Pd.

●Operating Conditions (Ta=25℃)

Parameter	Symbol	Ratings		Unit
		Min.	Max.	
Input Voltage 1	V_{CC}	4.5	5.5	V
Input Voltage 2	V_{DD}	4.5	5.5	V
Input Voltage 3	V_{IN}	3.0	28	V
BOOT Voltage	$V_{BOOT1/2}$	4.5	30	V
SW Voltage	$V_{SW1/2}$	-2	33	V
BOOT-SW Voltage	V_{HG1}-V_{SW1}, V_{HG2}-V_{SW2}	4.5	5.5	V
Logic Input Voltage	$V_{EN1/2}$	0	5.5	V
Setting Voltage for Output Voltage	$V_{REF1/2}$	0.7	2.0	V
Is Input Voltage	$V_{Is+1/2}$, $V_{Is-1/2}$	0.7	2.0	V
MIN ON time	tonmin	-	100	nsec

★ This product should not be used in a radioactive environment.

●Electrical Characteristics (unless otherwise noted, Ta=25℃ V_{CC}=5V,V_{DD}=5V,V_{EN}=3V,V_{IN}=12V,V_{REF}=1.8V,R_{FS}=68kΩ)

Parameter	Symbol	Limits			Unit	Conditions
		MIN.	TYP.	MAX.		
[Whole Device]						
VCC bias current	Icc	-	1.4	2.0	mA	
VIN bias current	IIN	-	200	400	μA	
VCC standby current	Istb	-	-	20	μA	$V_{EN}1$=$V_{EN}2$=0V
VIN standby current	IIN_Stb	-	20	40	μA	$V_{EN}1$=$V_{EN}2$=0V
EN Low voltage 1,2	VEN_low1,2	GND	-	0.8	V	
EN High voltage 1,2 (forced continuous mode)	VENth_con1,2	2.3	-	3.8	V	
EN High voltage 1,2 (SLLM™ mode)	VENth_sllm1,2	4.2	-	5.5	V	
EN bias current 1,2	I_{EN}1,2	-	7	10	μA	
VREG voltage	V_{REG}1,2	2.475	2.500	2.525	V	I_{REG}=500μA Ta=-10～100℃*2
[Under voltage lock out block]						
VCC threshold voltage	V_{CC_UVLO}	4.1	4.3	4.5	V	V_{CC}:Sweep up
VCC hysteresis voltage	dV_{CC}_UVLO	100	160	220	mV	V_{CC}:Sweep down
VIN threshold voltage	V_{IN}_UVLO	2.4	2.6	2.8	V	V_{IN}:Sweep up
VIN hysteresis voltage	dV_{IN}_UVLO	100	160	220	mV	V_{IN}:Sweep down
VREG threshold voltage	V_{REG}_UVLO	2.0	2.2	2.4	V	V_{REG}:Sweep up
VREG hysteresis voltage	dV_{REG}_UVLO	100	160	220	mV	V_{REG}:Sweep down
[Over Voltage Protection block]						
VOUT threshold voltage 1,2	V_{OUT}_OVP1,2	V_{REF} ×1.15	V_{REF} ×1.20	V_{REF} ×1.25	V	
[Power Good block]						
V_{OUT} Power Good Low voltage 1,2	V_{PGOOD}_low1,2	V_{REF} ×0.87	V_{REF} ×0.90	V_{REF} ×0.93	V	
V_{OUT} Power Good High voltage 1,2	V_{PGOOD}_high1,2	VREF ×1.07	VREF ×1.10	VREF ×1.13	V	
Discharge ON resistance 1,2	Ron_{PGOOD}1,2	-	1.0	2.0	kΩ	
Delay time 1,2	T_{PGOOD}1,2	150	250	350	μsec	

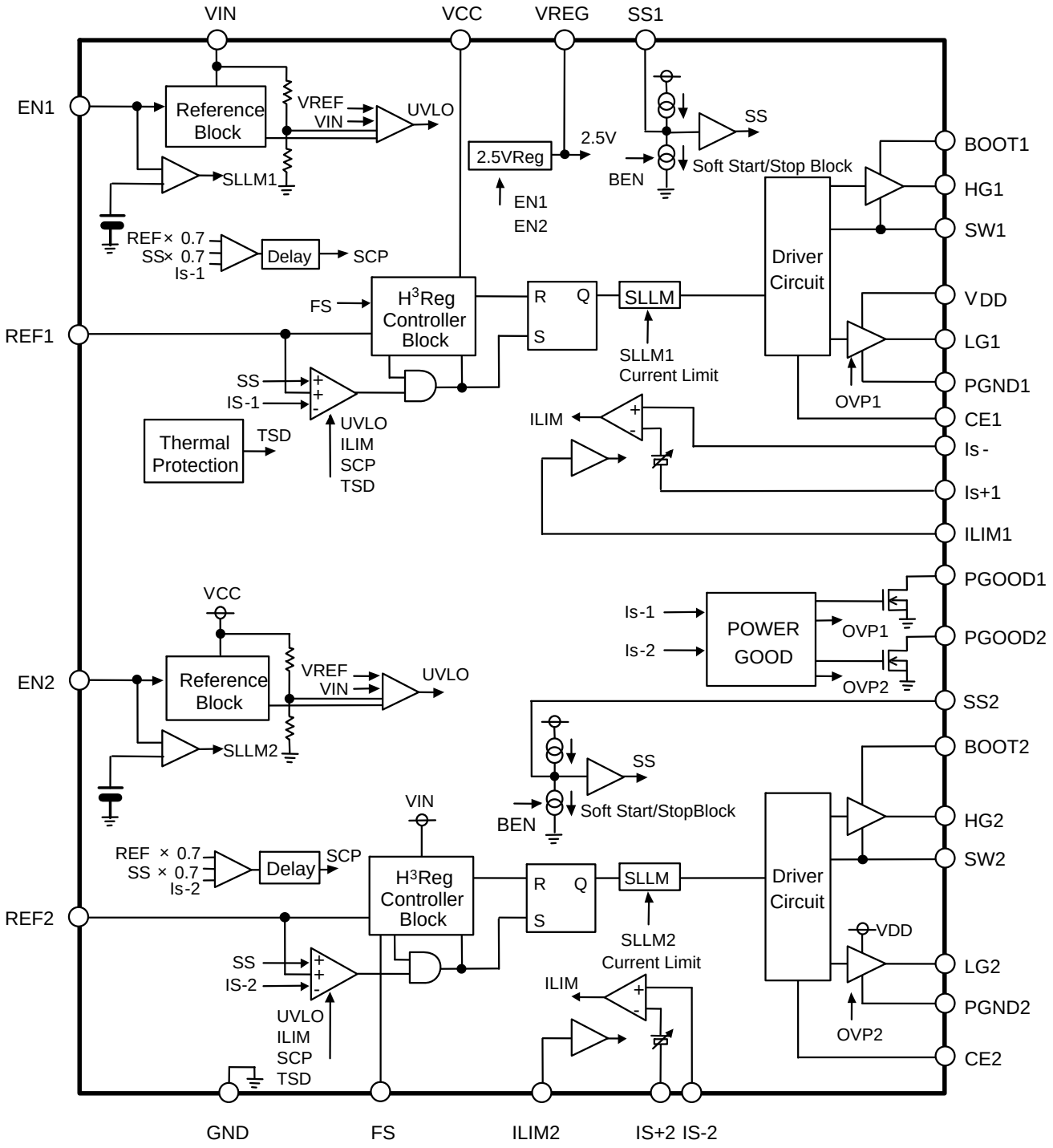
*2 Designed guarantee

●Electrical Characteristics (unless otherwise noted, Ta=25℃ V_{CC}=5V,V_{DD}=5V,V_{EN}=3V,V_{IN}=12V,V_{REF}=1.8V,R_{FS}=68kΩ)

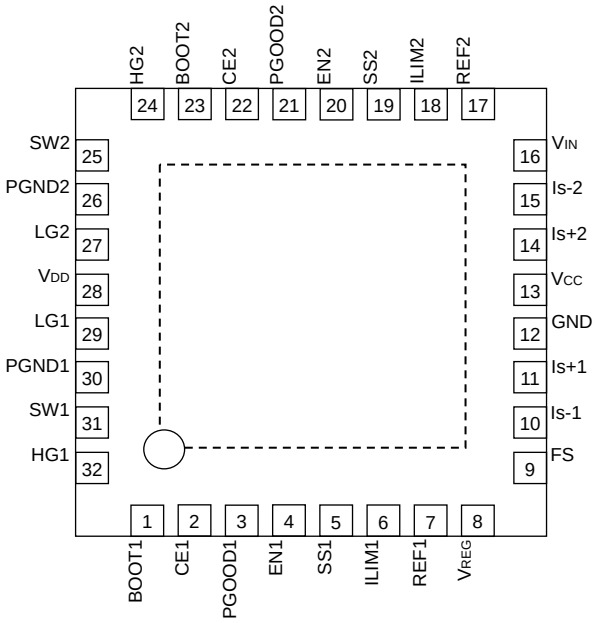
Parameter	Symbol	Limits			Unit	Conditions
		MIN.	TYP.	MAX.		
[H^3REG^{TM} Control block]						
ON Time1	t_{on1}	400	500	600	nsec	RFS=68kΩ
MAX ON Time 1	T_{onmax1}	2.5	3.0	3.5	μsec	
MIN OFF Time 1	$T_{offmin1}$	500	600	700	nsec	
ON Time 2	ton2	250	350	450	nsec	R_{FS}=68kΩ
MAX ON Time 2	T_{onmax2}	2.5	3.0	3.5	μsec	
MIN OFF Time 2	$T_{offmin2}$	500	600	700	nsec	
[FET Driver block]						
HG upper side ON resistance 1,2	R_{HG}hon1,2	-	3.0	6.0	Ω	
HG lower side ON resistance 1,2	R_{HG}lon1,2	-	2.0	4.0	Ω	
LG upper side ON resistance 1,2	R_{LG}hon1,2	-	2.0	4.0	Ω	
LG lower side ON resistance 1,2	R_{LG}lon1,2	-	0.5	1.0	Ω	
[Soft Start block]						
Charge current	I_{SS}_char1,2	1.5	2	2.5	μA	
Discharge current	I_{SS}_dis1,2	1.5	2	2.5	μA	
Discharge threshold voltage	V_{SS}_disth1,2	-	0.1	0.2	V	
Standby voltage	V_{SS}_STB1,2	-	-	50	mV	
[Current Limit block]						
Current limit threshold voltage 1_1,2	V_{llim1}1,2	40	50	60	mV	V_{ILIM}=0.5V
Current limit threshold voltage 2_1,2	V_{llim2}1,2	170	200	230	mV	V_{ILIM} =2.0V
Reflux current limit threshold voltage1_1,2	$V_{Rellim1}$1,2	-60	-50	-40	mV	V_{ILIM} =0.5V
Reflux current limit threshold voltage2_1,2	$V_{Rellim2}$1,2	-230	-200	-170	mV	V_{ILIM} =2.0V
[Output Voltage Sense block]						
V_{IS} offset voltage1,2	V_{IS_off}1,2	V_{REF} -3m	V_{REF}	V_{REF} +3m	V	Ta=-10～100℃*2
REF bias current1,2	I_{REF}1,2	-100	0	100	nA	
Is+ input current1,2	I_{Is+}1,2	-100	0	100	nA	V_{Is+}=1.8V
Is- input current1,2	I_{Is-}1,2	-100	0	100	nA	V_{Is-}=1.8V
[SCP block]						
Threshold voltage 1,2	Vthscp1,2	-	V_{REF}×0.7	-	V	
Delay time 1,2	tscp1,2	0.7	1	1.3	msec	

*2 Designed guarantee

●Block Diagram



●Pin Configuration



●Pin Function Table

PIN No.	PIN name	PIN function
1	BOOT1	HG driver power supply pin 1
2	CE1	Reactive pin 1 for lower ESR output capacitor
3	PGOOD1	Power good signal output pin 1
4	EN1	Enable input pin 1 (0～0.8V:OFF, 2.3～3.8V:continuous mode, 4.2～5.5V:SLLM™)
5	SS1	Connective pin 1 of capacitor for soft start/soft stop
6	ILIM1	Current limitsetting pin 1
7	REF1	Output voltage setting pin 1
8	VREG	Reference voltage inside IC (Output : 2.5V)
9	FS	Resistance connective pin for setting frequency
10	Is-1	Current sense pin- 1
11	Is+1	Current sense pin+ 1
12	GND	Sense GND
13	VCC	Power supply input pin
14	Is+2	Current sense pin+ 2
15	Is-2	Current sense pin- 2
16	VIN	Battery voltage sense pin
17	REF2	Output voltage setting pin 2
18	ILIM2	Current limit setting pin 2
19	SS2	Connective pin 2 of capacitor for soft start/soft stop
20	EN2	Enable input pin 2 (0～0.8V:OFF, 2.3～3.8V:continuous mode, 4.2～5.5V:SLLM™)
21	PGOOD2	Power good signal input pin 2
22	CE2	Reactive pin 2 for lower ESR output capacitor
23	BOOT2	HG driver power supply pin 2
24	HG2	High side FET gate drive pin 2
25	SW2	High side FET source pin 2
26	PGND2	Power GND2
27	LG2	Low side FET gate drive pin 2
28	VDD	Power supply input pin
29	LG1	Low side FET gate drive pin 1
30	PGND1	Power GND 1
31	SW1	High side FET source pin 1
32	HG1	High side FET gate drive pin 1
reverse	FIN	substrate

●Reference Data

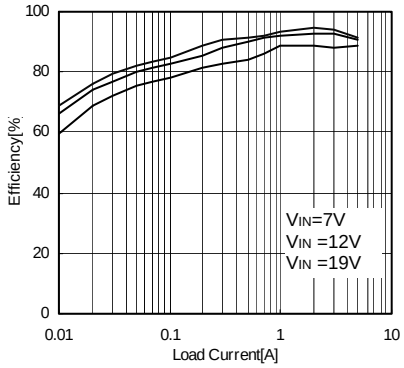


Fig.1 Io-efficiency (SLLM™)

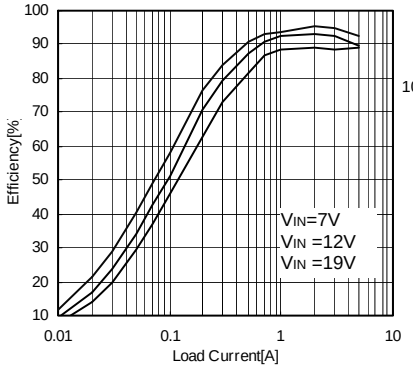


Fig.2 Io- efficiency (Continuous mode)

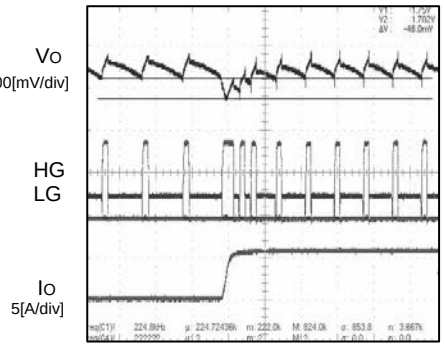


Fig.3 Transitional response (Io=0→5A) (Continuous mode)

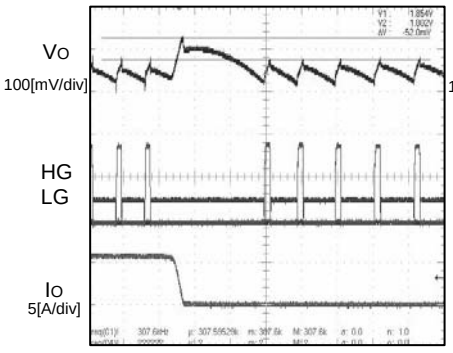


Fig.4 Transitional response (Io=5→0A) (Continuous mode)

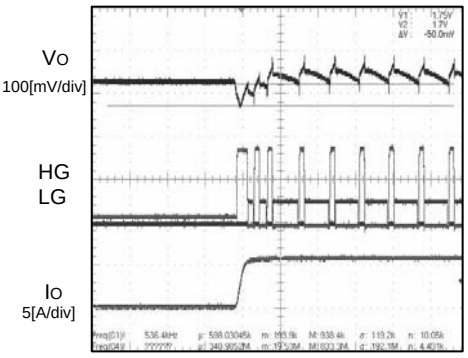


Fig.5 Transitional response (Io=0→5A) (SLLM™)

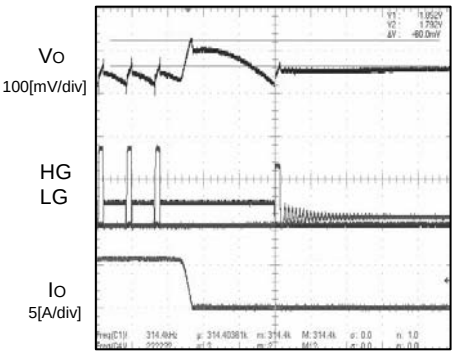


Fig.6 Transitional response (Io=5→0A) (SLLM™)

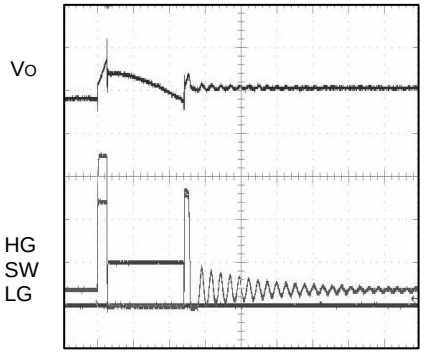


Fig.7 SLLM™ : Io=0A

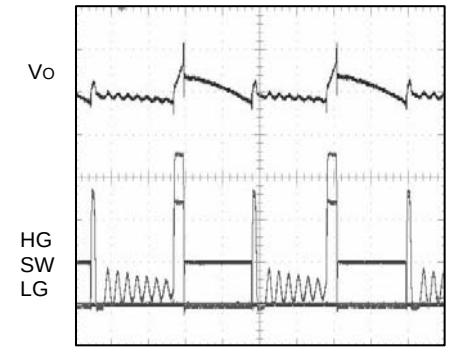


Fig.8 SLLM™ : Io=0.4A

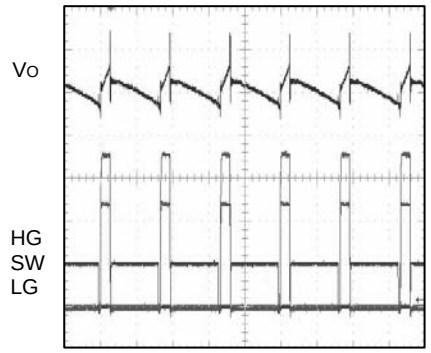


Fig.9 SLLM™ : Io=1A

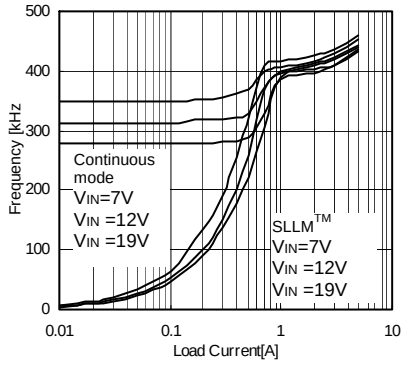


Fig.10 Io-Frequency

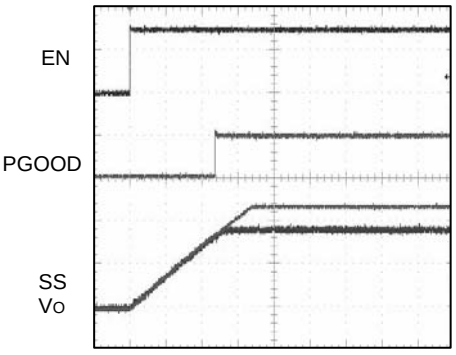


Fig.11 starting wave

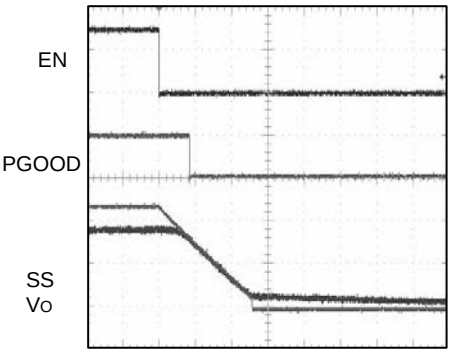
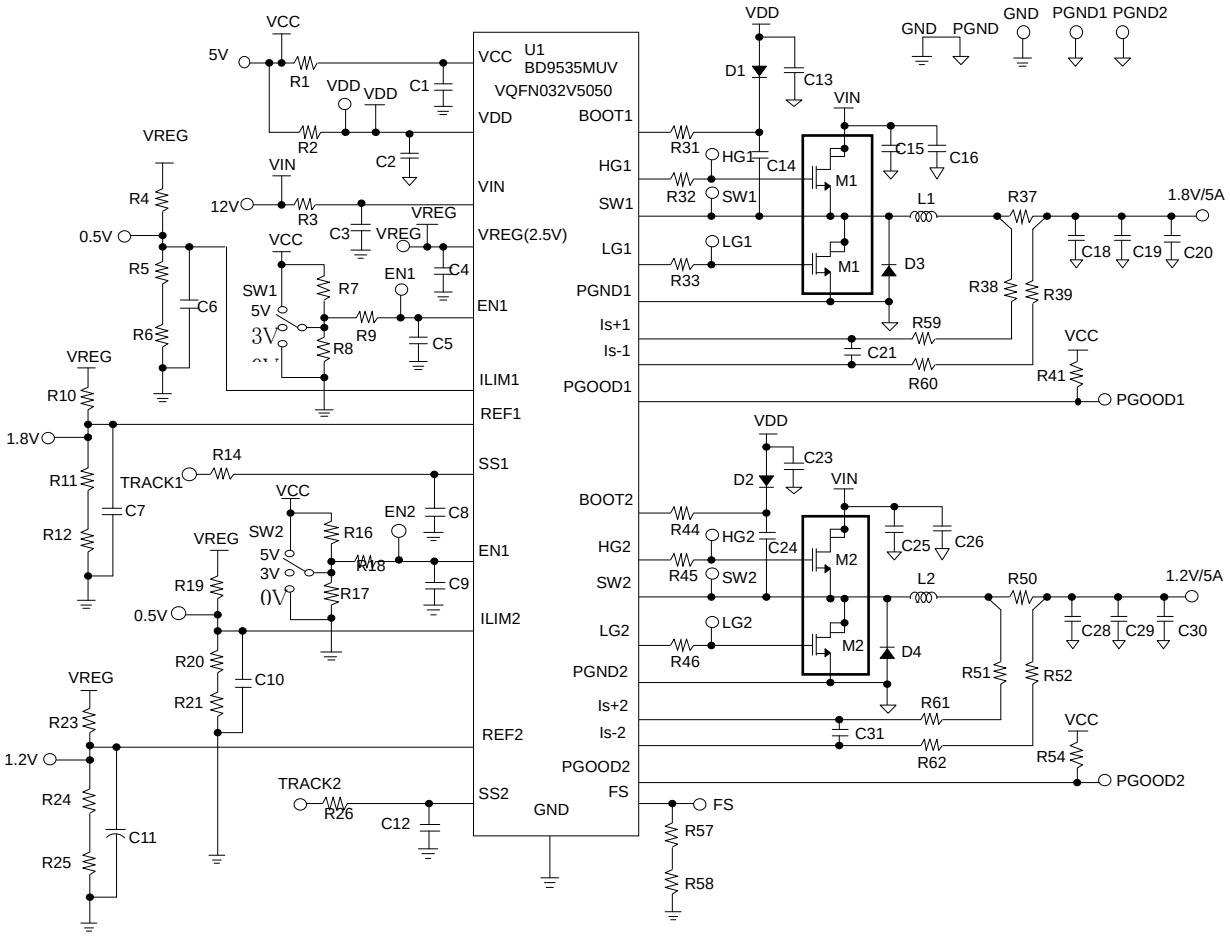


Fig.12 stopping wave

●Evaluation Board Circuit



●Evaluation Board Parts List

Part No	Value	Company	Parts Name
R1	10Ω	ROHM	MCR03EZPF10R0
R2	0Ω	ROHM	MCR03EZHJ000
R3	1kΩ	ROHM	MCR03EZPF1001
R4	200kΩ	ROHM	MCR03EZPF2003
R5	51kΩ	ROHM	MCR03EZPF5102
R6	0Ω	ROHM	MCR03EZHJ000
R7	51kΩ	ROHM	MCR03EZPF5102
R8	91kΩ	ROHM	MCR03EZPF9102
R9	0Ω	ROHM	MCR03EZHJ000
R10	22kΩ	ROHM	MCR03EZPF2202
R11	56kΩ	ROHM	MCR03EZPF5602
R12	0Ω	ROHM	MCR03EZHJ000
R14	10kΩ	ROHM	MCR03EZPF1002
R16	51kΩ	ROHM	MCR03EZPF5102
R17	91kΩ	ROHM	MCR03EZPF9102
R18	0Ω	ROHM	MCR03EZHJ000
R19	200kΩ	ROHM	MCR03EZPF2003
R20	51kΩ	ROHM	MCR03EZPF5102
R21	0Ω	ROHM	MCR03EZHJ000
R23	39kΩ	ROHM	MCR03EZPF3902
R24	36kΩ	ROHM	MCR03EZPF3602
R25	0Ω	ROHM	MCR03EZHJ000
R26	10kΩ	ROHM	MCR03EZPF1002
R31	0Ω	ROHM	MCR03EZHJ000
R32	0Ω	ROHM	MCR03EZHJ000
R33	0Ω	ROHM	MCR03EZHJ000
R37	7mΩ	ROHM	PMR100HZPFU7L00
R38	0Ω	ROHM	MCR03EZHJ000
R39	0Ω	ROHM	MCR03EZHJ000
R41	100kΩ	ROHM	MCR03EZPF1003
R44	0Ω	ROHM	MCR03EZHJ000
R45	0Ω	ROHM	MCR03EZHJ000
R46	0Ω	ROHM	MCR03EZHJ000
R50	7mΩ	ROHM	PMR100HZPFU7L00
R51	0Ω	ROHM	MCR03EZHJ000
R52	0Ω	ROHM	MCR03EZHJ000

Part No	Value	Company	Parts Name
R54	100kΩ	ROHM	MCR03EZPF1003
R57	75kΩ	ROHM	MCR03EZPF7502
R58	0Ω	ROHM	MCR03EZHJ000
R59	100Ω	ROHM	MCR03EZPF1000
R60	100Ω	ROHM	MCR03EZPF1000
R61	100Ω	ROHM	MCR03EZPF1000
R62	100Ω	ROHM	MCR03EZPF1000
C1	10µF	MURATA	GRM21 Series
C2	10µF	MURATA	GRM21 Series
C3	0.01µF	MURATA	GRM18 Series
C4	1µF	KYOCERA	CM105B105K06A
C6	0.1µF	MURATA	GRM18 Series
C7	0.1µF	MURATA	GRM18 Series
C8	0.047µF	MURATA	GRM18 Series
C10	0.1µF	MURATA	GRM18 Series
C11	0.1µF	MURATA	GRM18 Series
C12	0.047µF	MURATA	GRM18 Series
C13	10µF	KYOCERA	CM21B106M06A
C14	0.1µF	MURATA	GRM18 Series
C15	10µF(25V)	KYOCERA	CT32X5R106K25A
C18	200µF	SANYO	2R5TPE220MF
C21	100pF	MURATA	GRM18 Series
C23	10µF	KYOCERA	CM21B106M06A
C24	0.1µF	MURATA	GRM18 Series
C26	10µF(25V)	KYOCERA	CT32X5R106K25A
C28	200µF	SANYO	2R5TPE220MF
C31	100pF	MURATA	GRM18 Series
D1	-	ROHM	RB521S-30
D2	-	ROHM	RB521S-30
D3	-	ROHM	RSX501L-20
D4	-	ROHM	RSX501L-20
L1	2.5µH	Sumida	CDEP105-2R5MC-32
L2	2.5µH	Sumida	CDEP105-2R5MC-32
M1	-	ROHM	SH8K4(2in1)
M2	-	ROHM	SH8K4(2in1)
U1	-	ROHM	BD9535MUV

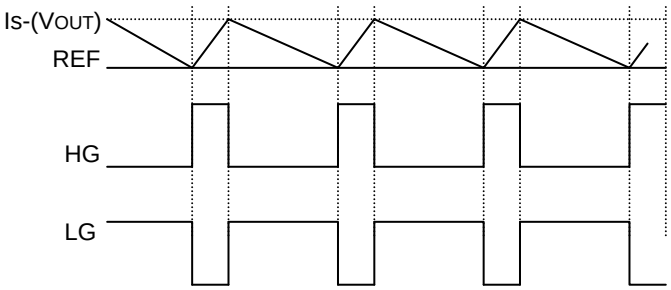
●Pin Descriptions

- VCC (13pin)
  This is the power supply pin for IC internal circuits, except the FET driver. The maximum circuit current is 2.0mA. The input supply voltage range is 4.5V to 5.5V. It is recommended that a 0.1µF bypass capacitor be put in this pin.
- EN1/EN2 (4pin/20pin)
  When EN pin voltage is at least 2.3V, the status of this switching regulator become active. Conversely, the status switches off when EN pin voltage goes lower than 0.8V and circuit current becomes 20µA or less. This pin is also switch pin of SLLM™. The voltage is 2.3V to 3.8V : forced continuous mode, 4.2V to 5.5V : SLLM™. These operating modes are changeable to control by power supply system 3.3V or 5V.
- VDD (28pin)
  This is the power supply pin to drive the LOW side FET. It is recommended that a 1µF bypass capacitor be established to compensate for rush current during the FET ON/OFF transition.
- VREG (8pin)
  This is the reference voltage output pin. The voltage is 2.5V, with 100µA current ability. It is recommended that a 1µF capacitor be established between VREF and GND. It is available to set VREF by the resistance division value from VREG in case VREF is not set from an external power supply.
- REF1/REF2 (7pin/17pin)
  This is the setting pin for output voltage of switching regulator. It is so convenient to be synchronized to outside power supply. This IC controls the voltage in the status of VREF1≒Vis-1 or VREF2≒Vis-2.
- ILIM1/ILIM2 (6pin/18pin)
  BD9535MUV detects the voltage between Is+ pin and Is- pin and limits the output current (OCP). Voltage equivalent to 1/10 of the ILIM voltage is the voltage drop of external current sense resistor. A very low current sense resistor or inductor DCR can also be used for this platform.
- SS1/SS2 (5pin/19pin)
  This is the adjustment pin to set the soft start/stop time. SS voltage is low during standby status. When EN is ON, the soft start time can be determined by the SS charge current and capacitor between SS-GND. Until SS reaches REF voltage, the output voltage is equivalent to SS voltage.
- VIN (16pin)
  The duty cycle is determined by input voltage and controls output voltage. In other words, the output voltage is affected by input voltage. Therefore, when VIN voltage fluctuates, the output voltage becomes also unstable. Since the VIN line is also the input voltage of the switching regulator, stability depends on the impedance of the voltage supply. It is recommended to establish a bypass capacitor or CR filters suitable for the actual application.
- FS (9pin)
  This is the pin to adjust the switching frequency with the resistor. The frequency range is from 200 kHz to 600 kHz.
- Is+1/Is+2,Is-1/Is-2 (11pin/14pin/10pin/15pin)
  These pins are connected to both sides of the current sense resistor to detect output current. The voltage drop between Is+ and Is- is compared with the voltage equivalent to 1/10 of ILIM voltage. When this voltage drop hits the specified voltage level, the output voltage is OFF.
- BOOT1/BOOT2 (1pin/23pin)
  This is the voltage supply to drive the high side FET. The maximum absolute ratings are 35V (from GND) and 7V (from SW). BOOT voltage swings between (VIN+Vcc) and Vcc during active operation.
- HG1/HG2 (29pin/27pin)
  This is the voltage supply to drive the Gate of the high side FET. This voltage swings between BOOT and SW. High-speed Gate driving for the high side FET is achieved due to the low on-resistance (3 ohm when HG is high, 2 ohm when HG is low) driver.
- SW1/SW2 (31pin/25pin)
  This is the source pin for the high side FET. The maximum absolute ratings are 30V (from GND). SW voltage swings between VIN and GND.
- LG1/LG2 (29pin/27pin)
  This is the voltage supply to drive the Gate of the low side FET. This voltage swings between VDD and PGND. High-speed Gate driving for the low side FET is achieved due to the low on-resistance (3 ohm when LG is high, 0.5 ohm when LG is low) driver.
- PGND1/PGND2 (30pin/26pin)
  This is the power ground pin connected to the source of the low side FET. This is the source pin for low-side FET. It is prepared for each channel to reduce the interference among channels.
- PGOOD1/PGOOD2 (3pin/21pin)
  This is the monitor pin for output voltage (Is-1/Is-2). When the output voltage is within 10% of setting voltage (REF1/2), High is output. It is open drain pin and connects to other power supply through the pull-up resistance.
- CE1/PCE2 (2pin/22pin)
  This pin is helpful for using ceramic capacitor as output capacitor. It is stable to use low ESR capacitor (small ripple voltage).
- GND (12pin)
  This is GND pin for Analog and Digital series. Set the reverse side of IC equivalent to the voltage of this pin.

●Explanation of Operation

The BD9535MUV is a 2ch synchronous buck regulator controller incorporating ROHM's proprietary H^{3}REG^{TM} CONTROLLA control system. When VOUT drops due to a rapid load change, the system quickly restores VOUT by extending the TON time interval. Thus, it serves to improve the regulator's transient response. Activating the Light Load Mode will also exercise Simple Light Load Mode (SLLM^{TM}) control when the load is light, to further increase efficiency.

H^{3}Reg^{TM} control
(Normal operation)

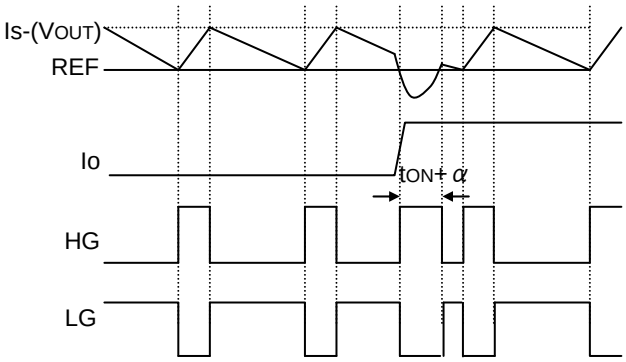


When VOUT falls to a threshold voltage (REF), the drop is detected, activating the H^{3}REG^{TM} CONTROLLA system.

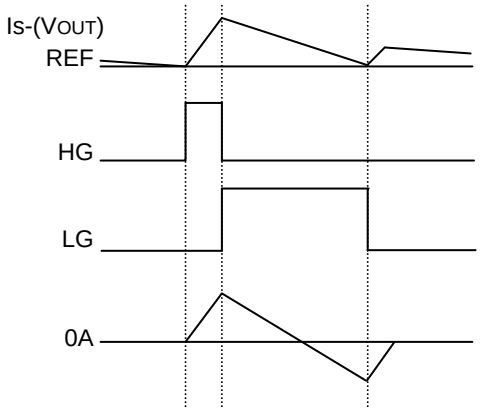
$$t_{ON} = \frac{REF}{V_{IN}} \times \frac{1}{f} \text{ [sec]} \cdots (1)$$

HG output is determined by the formula above.

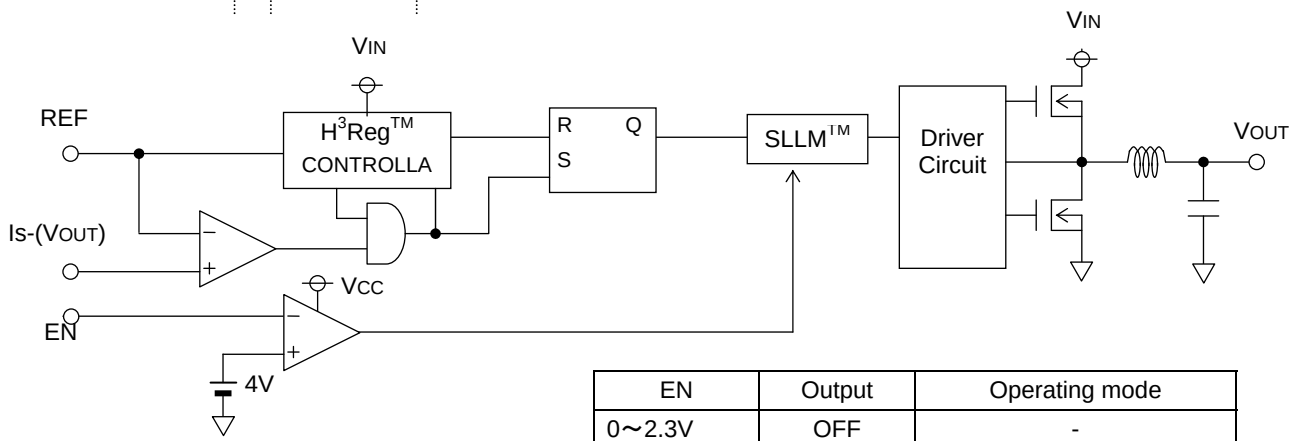
(VOUT drops due to a rapid load change)



When VOUT drops due to a rapid load change, and the voltage remains below REF after the programmed tON time interval has elapsed, the system quickly restores VOUT by extending the tON time, improving the transient response.



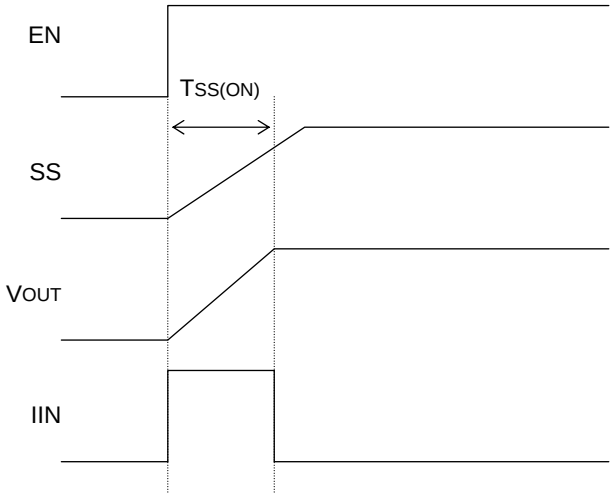
In SLLM (SLLM=0V), SLLM function is operated when LG pin is OFF and the coil current is lower than 0A
(the current goes from VOUT to SW). And it stops to output next HG.
When VOUT goes lower than REF voltage again, the status of HG is ON.



EN	Output	Operating mode
0～2.3V	OFF	-
2.3～3.8V	ON	Forced continuous mode
4.2～5.5V	ON	SLLM^{TM}

●Timing Chart

・Soft Start Function



Soft start is exercised with the EN pin set high. Current control takes effect at startup, enabling a moderate output voltage “ramping start.” Soft start timing and incoming current are calculated with formulas (2) and (3) below.

Soft start time

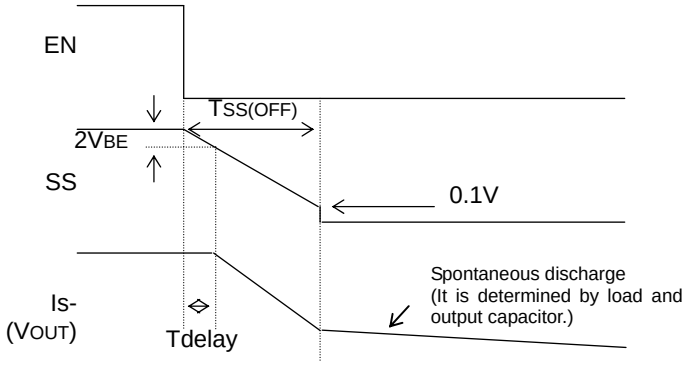
$$T_{SS(ON)} = \frac{REF \times Css}{2\mu A(typ)} \quad [sec] \quad \cdot\cdot\cdot (2)$$

rush current

$$I_{IN} = \frac{Co \times V_{OUT}}{Tss} \quad [A] \quad \cdot\cdot\cdot (3)$$

(Css: Soft start capacitor; Co: Output capacitor)

・Soft Stop Function



Soft stop is exercised with the EN pin set low. Current control takes effect at startup, enabling a moderate output voltage. Soft start timing and incoming current are calculated with formulas (4) below.

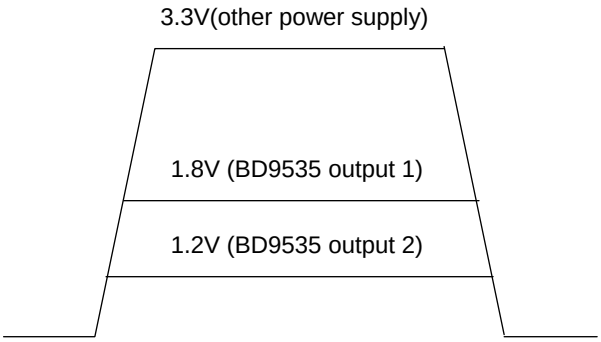
Soft stop time

$$T_{SS(OFF)} = \frac{(REF+2V_{BE}-0.1) \times Css}{2\mu A(typ)} \quad [sec] \quad \cdot\cdot\cdot (4)$$

V_{BE} = 0.6[V] (typ)

$$Tdelay = \frac{2V_{BE} \times C_{SS}}{2\mu A(typ)} \quad [sec] \quad \cdot\cdot\cdot (5)$$

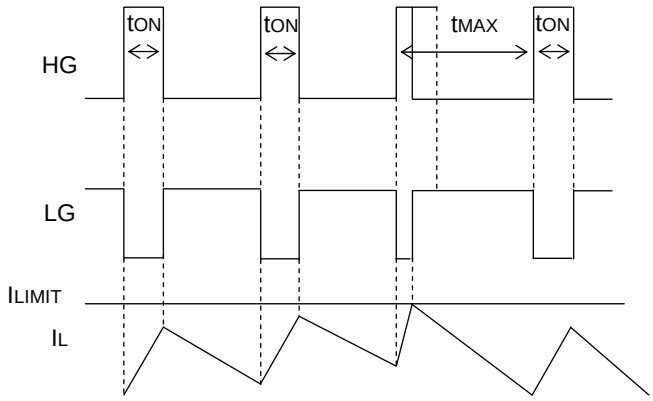
・Synchronous operation with other power supply



These power supply sequences are realized to connect SS pin to other power supply output through the resistance (10kΩ).

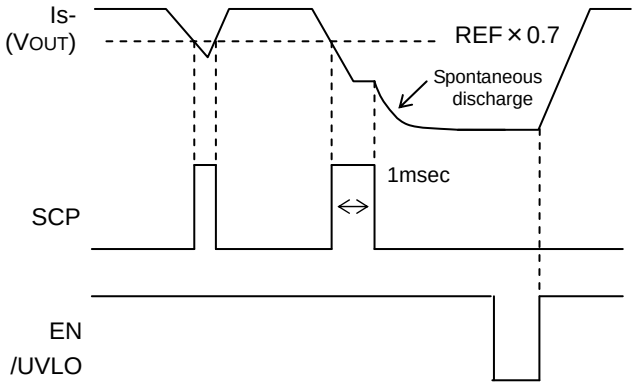
●Timing chart

・Over current protection circuit



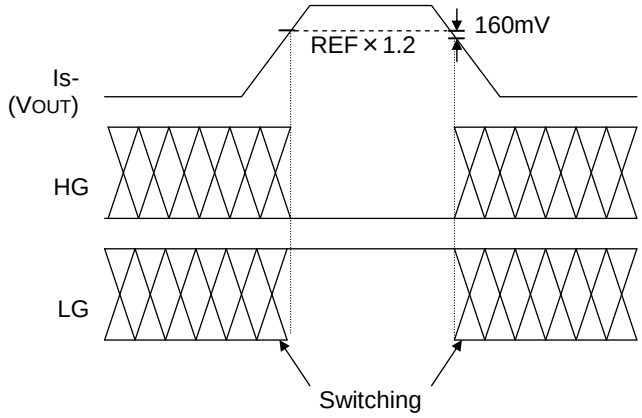
During the normal operation, when VOUT becomes less than REF Voltage, HG becomes High during the time TON. However, when inductor current exceeds I_{LIMIT} threshold, HG becomes OFF.
After MAX ON TIME, HG becomes ON again if the output voltage is lower than the specific voltage level and I_L is lower than I_{LIMIT} level.

・Timer Latch Type Short Circuit Protection



When output voltage (Is-) falls to REF × 0.7 or less, SCP comparator inside IC is exercised.
If the status of High is continued 1ms or more (programmed time inside IC), the IC goes OFF. It can be restored either by reconnecting the EN pin or disabling UVLO.

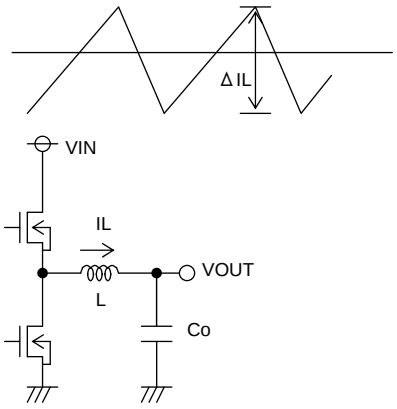
・Output Over Voltage Protection



When output rise to or above REF × 1.2, output over voltage protection is exercised, and low side FET goes up maximum for reducing output. (LG=High, HG=Low). When output falls, it returns to the standard mode.

●External Component Selection

1. Inductor (L) selection



Output ripple current

The inductor value is a major influence on the output ripple current. As formula (5) below indicates, the greater the inductor or the switching frequency, the lower the ripple current.

$$\Delta I_L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f} \quad [A] \cdots (6)$$

The proper output ripple current setting is about 30% of maximum output current.

$$\Delta I_L = 0.3 \times I_{OUT}max. \quad [A] \cdots (7)$$

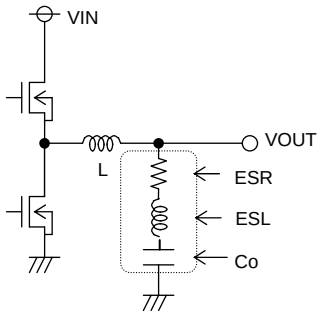
$$L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f} \quad [H] \cdots (8)$$

(ΔIL: output ripple current; f: switch frequency)

※Passing a current larger than the inductor's rated current will cause magnetic saturation in the inductor and decrease system efficiency. In selecting the inductor, be sure to allow enough margins to assure that peak current does not exceed the inductor rated current value.

※To minimize possible inductor damage and maximize efficiency, choose a inductor with a low (DCR, ACR) resistance.

2.Output Capacitor (C_O) Selection



Output capacitor

When determining the proper output capacitor, be sure to factor in the equivalent series resistance required to smooth out ripple volume and maintain a stable output voltage range.

Output ripple voltage is determined as in formula (9) below.

$$\Delta VOUT = \Delta IL \times ESR + ESL \times \Delta IL/T_{ON} \cdots (9)$$

(ΔIL: Output ripple current; ESR: CO equivalent series resistance, ESL: CO equivalent series inductance)

※ In selecting a capacitor, make sure the capacitor rating allows sufficient margin relative to output voltage. Note that a lower ESR can minimize output ripple voltage.

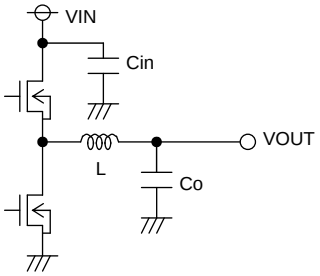
Please give due consideration to the conditions in formula (10) below for output capacity, bear in mind that output rise time must be established within the soft start time frame.

$$Co \leqq \frac{TSS \times (Limit - I_{OUT})}{VOUT} \cdots (10)$$

Tss: Soft start time
Limit: Over current detection
IOUT: Output current

Note: Improper capacitor may cause startup malfunctions.

3. Input Capacitor (Cin) Selection



Input Capacitor

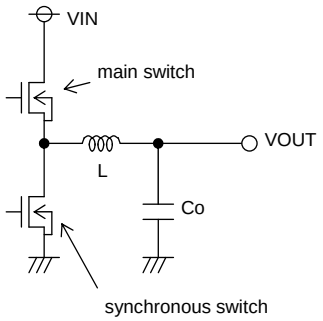
The input capacitor selected must have low enough ESR resistance to fully support large ripple output, in order to prevent extreme over current. The formula for ripple current IRMS is given in (11) below.

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{IN}-V_{OUT})}}{V_{IN}} \quad [A] \cdots (11)$$

Where $V_{IN} = 2 \times V_{OUT}$, $I_{RMS} = \frac{I_{OUT}}{2}$

A low ESR capacitor is recommended to reduce ESR loss and maximize efficiency.

4. MOSFET Selection



Loss on the main MOSFET

$P_{main}=P_{RON}+P_{GATE}+P_{TRAN}$

$$= \frac{V_{OUT}}{V_{IN}} \times R_{ON} \times I_{OUT}^2 + Qg \times f \times V_{DD} + \frac{V_{IN}^2 \times Crss \times I_{OUT} \times f}{I_{DRIVE}} \quad \cdot\cdot\cdot (12)$$

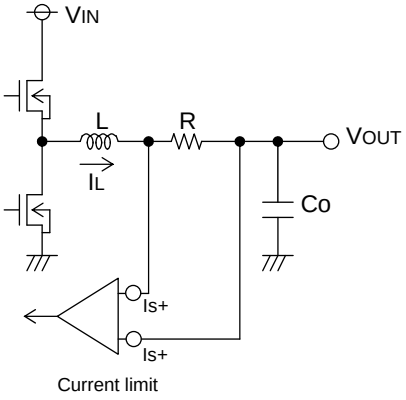
(Ron: On-resistance of FET; Qg: GATE total charge
f: Switching frequency, Crss: FET inverse transfer function;
I_{DRIVE}: Gate peak current)

Loss on the synchronous MOSFET

$P_{syn}=P_{RON}+P_{GATE}$

$$= \frac{V_{IN}-V_{OUT}}{V_{IN}} \times R_{ON} \times I_{OUT}^2 + Qg \times f \times V_{DD} \quad \cdot\cdot\cdot (13)$$

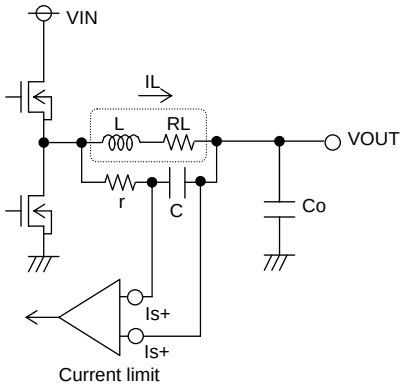
5. Setting Detection Resistance



The over current protection function detects the output ripple current peak value. This parameter (setting value) is determined as in formula (14) below.

$$I_{LMIT}= \frac{V_{ILIM} \times 0.1}{R} [A] \cdot\cdot\cdot (14)$$

(V_{ILIM}: ILIM voltage; R: Detection resistance)

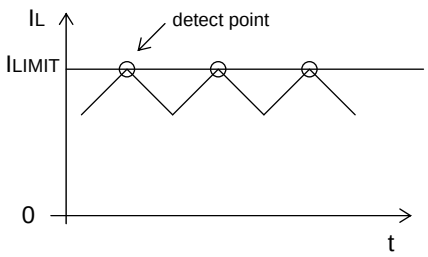


When the over current protection is detected by DCR of coil L, this parameter (setting value) is determined as in formula (14) below.

$$I_{LMIT}=V_{ILIM} \times 0.1 \times \frac{r \times C}{L} [A] \cdot\cdot\cdot (15)$$

$$(RL= \frac{L}{r \times C})$$

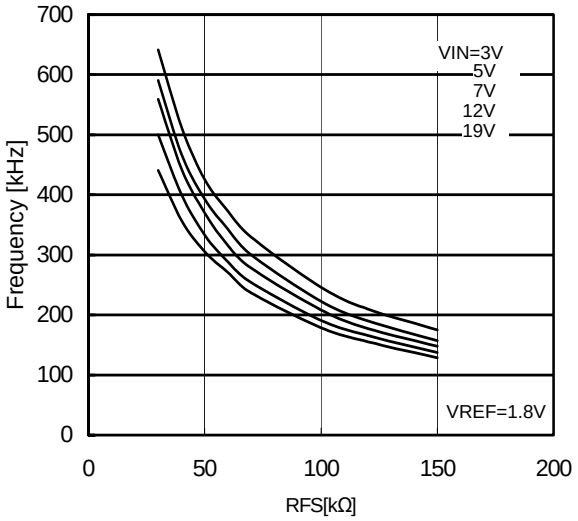
(V_{ILIM}:ILIM voltage RL: the DCR value of coil)



As soon as the voltage drop between Is+ and Is- generated by the inductor current becomes specific threshold, the gate voltage of the high side MOSFET becomes low.
Since the peak voltage of the inductor ripple current is detected, this operation can sense high current ripple operation caused by inductance saturated rated current and lead to high reliable systems.

6. Setting frequency

【1ch】

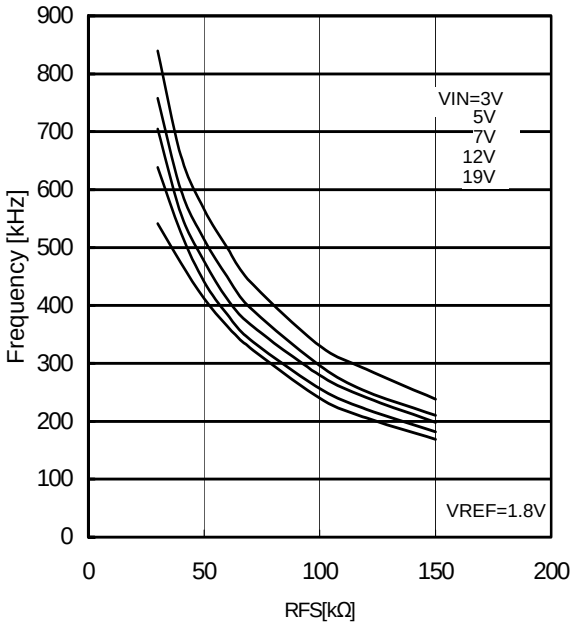


The On Time (T_{ON}) at steady state is determined by resistance value connected to FS pin.
But actually SW rising time and falling time come up due to influence of the external MOSFET gate capacity or switching speed and T_{ON} is increased.
The frequency is determined by the following formula after TON, input current and the REF voltage are fixed.

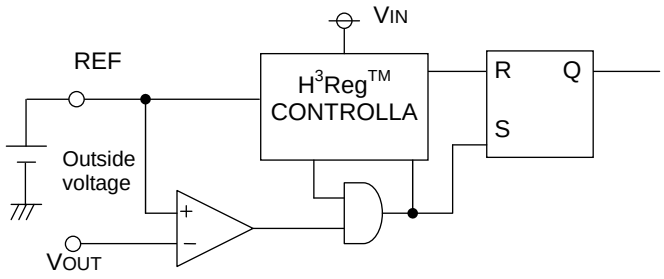
$$F = \frac{REF}{V_{IN} \times T_{ON}} \quad \cdots (15)$$

Consequently, total frequency becomes lower than the formula above.
T_{ON} is also influenced by Dead Time around the output current 0A area in continuous mode.
This frequency becomes lower than setting frequency.
It is recommended to check the steady frequency in large current area (at the point where the coil current doesn't back up).

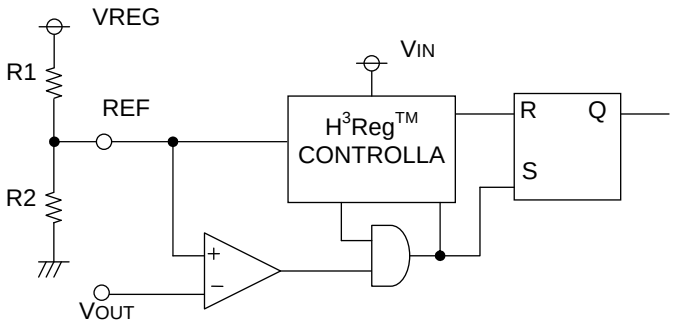
【2ch】



7. Setting standard voltage (REF)



It is available to synchronize setting the reference voltage (REF) with outside supply voltage [V] by using outside power supply voltage.



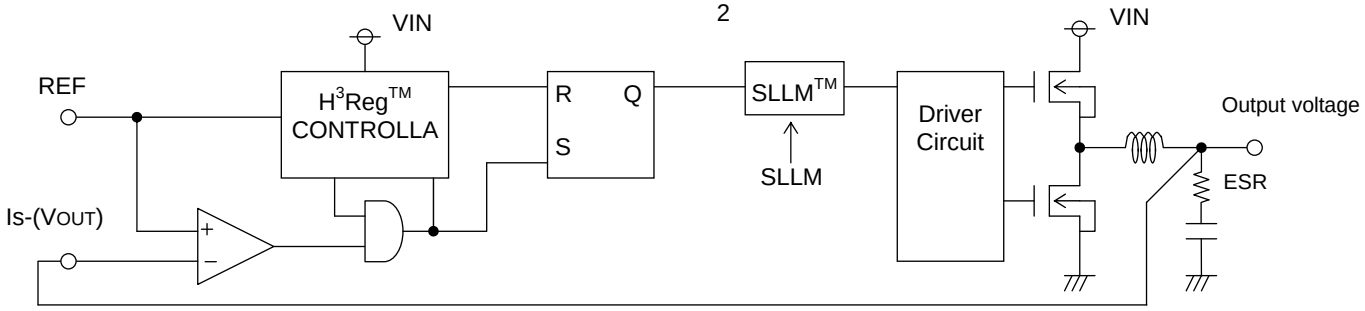
It is available to set the reference voltage (REF) by the resistance division value from VREG in case it is not set REF from an external power supply.

$$REF = \frac{R2}{R1+R2} \times VREG\ [V] \cdots (17)$$

8. Setting output voltage

This IC is operated that output voltage is REF≒Is-(V_{OUT}).
And it is operated that output voltage is feed back to FB pin in case the output voltage is 0.7V to 2.0V.
Actually, the average value of ripple voltage is added to output voltage.

$$\text{Output voltage} = REF + \frac{1}{2} \times \Delta IL \times ESR \cdots (18)$$



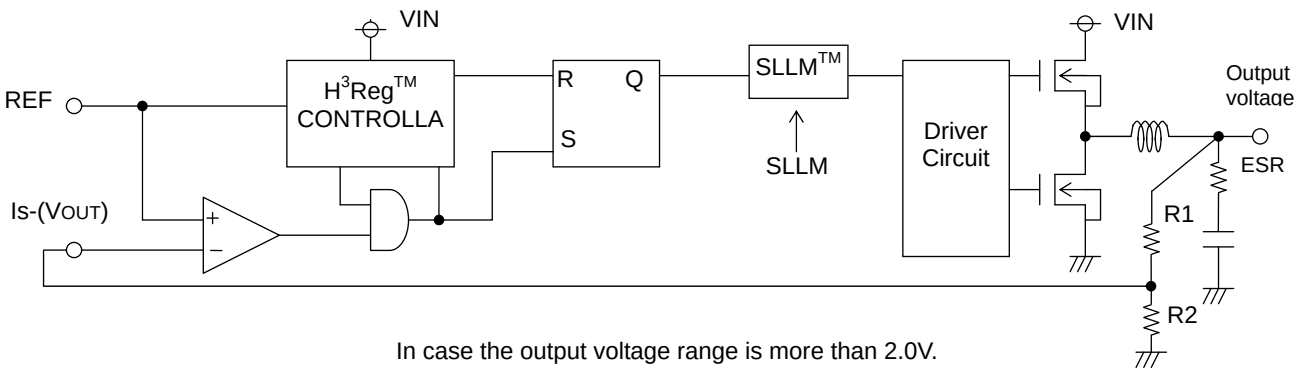
In case the output voltage range is 0.7V to 2.0V.

It is operated that the resistance division value of the output voltage is feed back to Is-pin in case the output voltage is more than 2.0V.

$$\text{output voltage} = \frac{R1+R2}{R2} \times REF + \frac{1}{2} \times \Delta IL \times ESR \cdots (19)$$

In this time, the frequency is also amplified by power of the resistance division. It is determined as in formula (20) below.

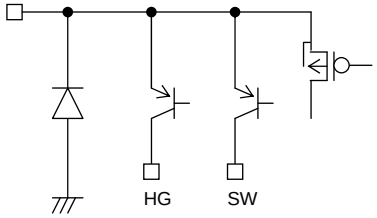
$$\text{Frequency} = \frac{R1+R2}{R2} \times (\text{frequency determined by REF})\ [Hz] \cdots (20)$$



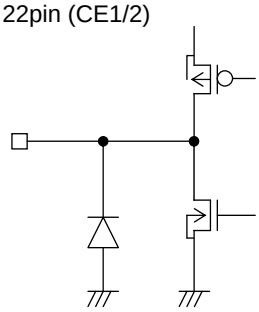
In case the output voltage range is more than 2.0V.

●I/O Equivalent Circuit

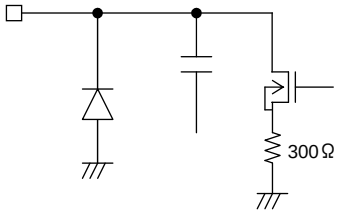
1pin, 23pin (BOOT1/2)



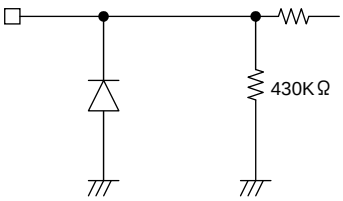
2pin, 22pin (CE1/2)



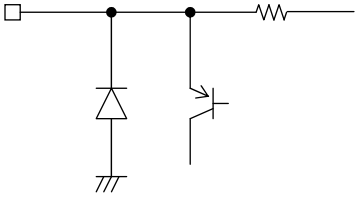
3pin, 21pin (PGOOD1/2)



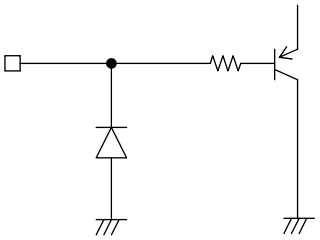
4pin, 20pin (EN1/2)



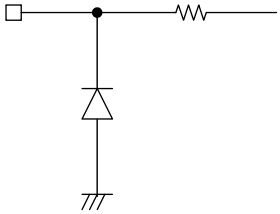
5pin, 19pin (SS1/2)



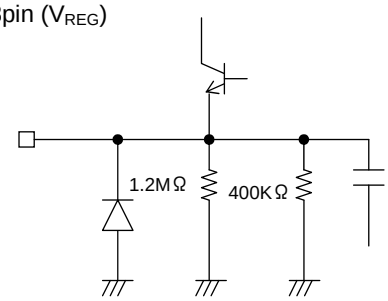
6pin, 18pin (ILIM1/2)



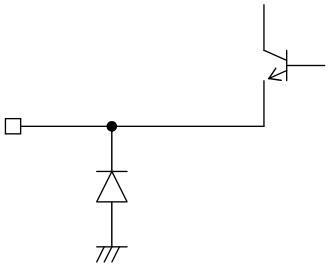
7pin, 17pin (REF1/2)



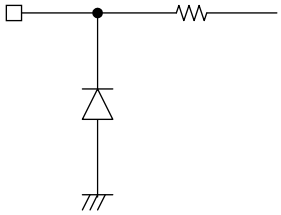
8pin (V_{REG})



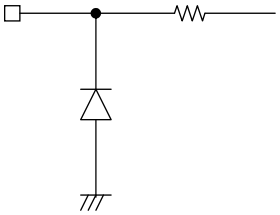
9pin (FS)



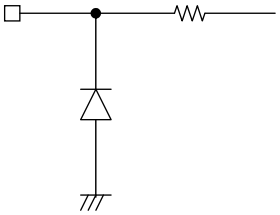
10pin, 15pin (Is-1/2)



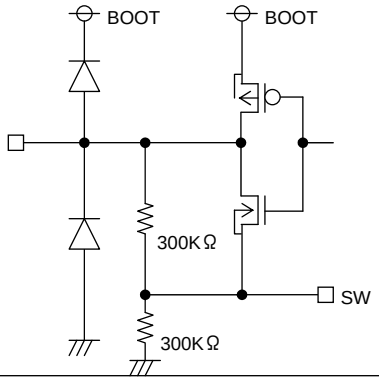
11pin, 14pin (Is+1/2)



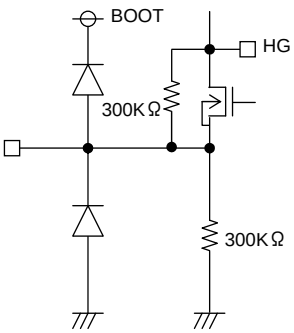
16pin (V_{IN})



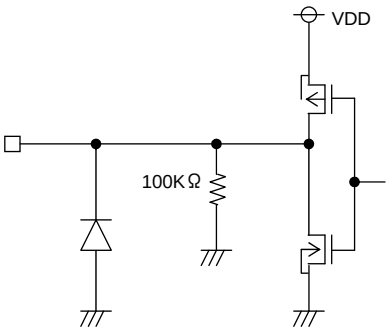
24pin, 32pin (HG1/2)



25pin, 31pin (SW1/2)



27pin, 29pin (LG1/2)



●Notes for use

1. Absolute maximum ratings
   An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. Connecting the power supply connector backward
   Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

3. Power supply lines
   Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

4. GND voltage
   The potential of GND pin must be minimum potential in all operating conditions.

5. Thermal design
   Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

6. Inter-pin shorts and mounting errors
   Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

7. Actions in strong electromagnetic field
   Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

8. ASO
   When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

9. Thermal shutdown circuit
   The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

	TSD on temperature [°C] (typ.)	Hysteresis temperature [°C] (typ.)
BD9535MUV	175	15

10. Testing on application boards
    When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

11. Regarding input pin of the IC
    This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:
    When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
    When GND > Pin B, the P-N junction operates as a parasitic transistor.
    Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

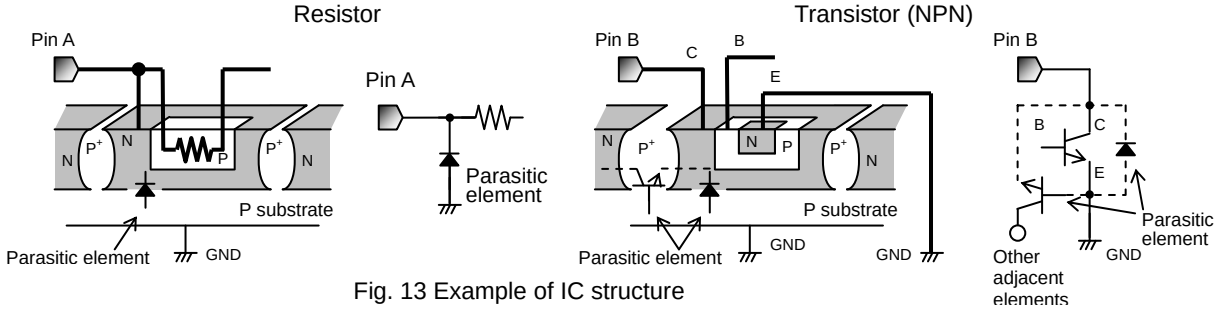
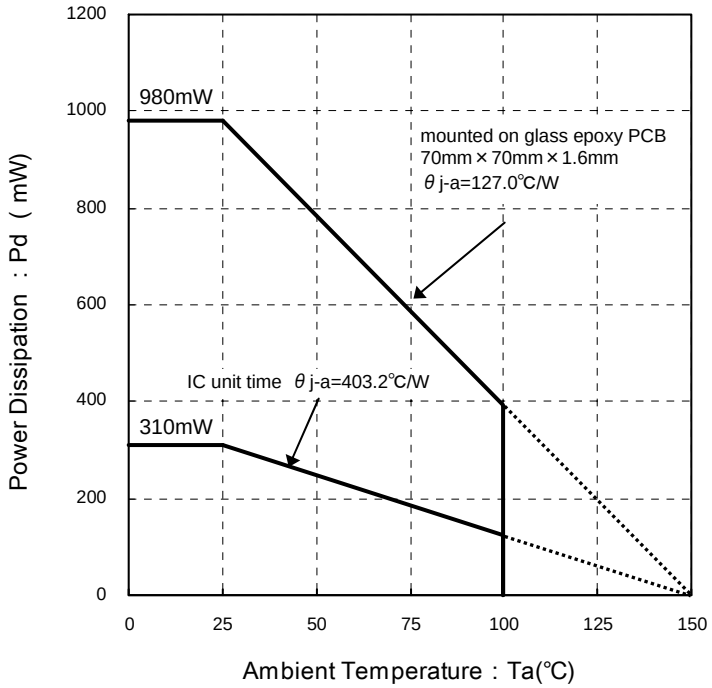


Fig. 13 Example of IC structure

12. Ground Wiring Pattern
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

●Power Dissipation

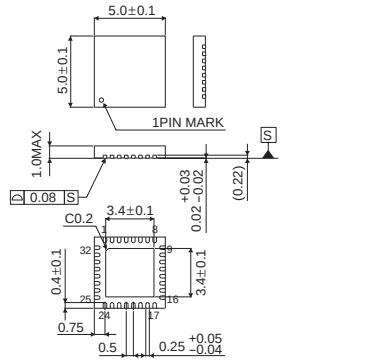


●Ordering part number

B	D	9	5	3	5	M	U	V	E	2

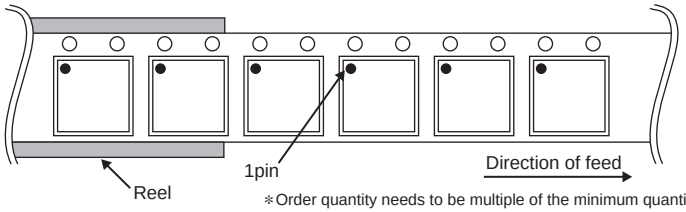
Part No. (BD) | Part No. (9535) | Package: MUV : VQFN032V5050 | Packaging and forming specification: E2: Embossed tape and reel

VQFN032V5050



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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