# Si5341/40 Rev D Data Sheet

## Low-Jitter, 10 or 4-Output, Any-Frequency, Any-Output Clock Generator

The any-frequency, any-output Si5341/40 clock generators combine a wide-band PLL with proprietary MultiSynth™ fractional synthesizer technology to offer a versatile and high performance clock generator platform. This highly flexible architecture is capable of synthesizing a wide range of integer and non-integer related frequencies up to 1 GHz on 10 differential clock outputs while delivering sub-100 fs rms phase jitter performance with 0 ppm error. Each of the clock outputs can be assigned its own format and output voltage enabling the Si5341/40 to replace multiple clock ICs and oscillators with a single device making it a true "clock tree on a chip."

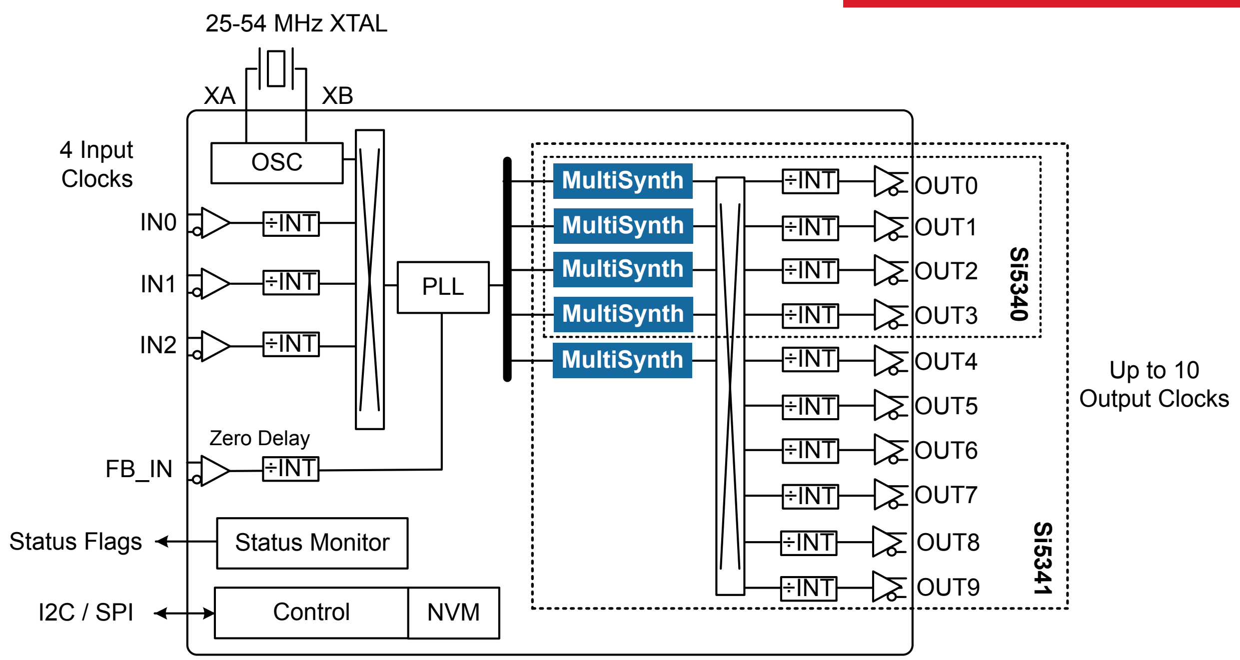
The Si5341/40 can be quickly and easily configured using ClockBuilderPro software. Custom part numbers are automatically assigned using a ClockBuilder Pro™ for fast, free, and easy factory pre-programming or the Si5341/40 can be programmed via I2C and SPI serial interfaces.

**Applications:**

- Clock tree generation replacing XOs, buffers, signal format translators
- Any-frequency clock translation
- Clocking for FPGAs, processors, memory
- Ethernet switches/routers
- OTN framers/mappers/processors
- Test equipment and instrumentation
- Broadcast video

**KEY FEATURES**

- Generates any combination of output frequencies from any input frequency
- Ultra-low jitter of 90 fs rms
- Input frequency range:
  - External crystal: 25 to 54 MHz
  - Differential clock: 10 to 750 MHz
  - LVCMOS clock: 10 to 250 MHz
- Output frequency range:
  - Differential: 100 Hz to 1028 MHz
  - LVCMOS: 100 Hz to 250 MHz
- Highly configurable outputs compatible with LVDS, LVPECL, LVCMOS, CML, and HCSL with programmable signal amplitude
- Si5341: 4 input, 10 output, 64-QFN 9x9 mm
- Si5340: 4 input, 4 output, 44-QFN 7x7 mm



# 1. Features List

The Si5341/40 Rev D features are listed below:

- Generates any combination of output frequencies from any input frequency
- Ultra-low jitter of 90 fs rms
- Input frequency range:
  - External crystal: 25 to 54 MHz
  - Differential clock: 10 to 750 MHz
  - LVCMOS clock: 10 to 250 MHz
- Output frequency range:
  - Differential: 100 Hz to 1028 MHz
  - LVCMOS: 100 Hz to 250 MHz
- Highly configurable outputs compatible with LVDS, LVPECL, LVCMOS, CML, and HCSL with programmable signal amplitude
- Locks to gapped clock inputs
- Optional zero delay mode
- Glitchless on the fly output frequency changes
- DCO mode: as low as 0.001 ppb steps
- Core voltage
  - VDD: 1.8 V ±5%
  - VDDA: 3.3 V ±5%
- Independent output clock supply pins
  - 3.3 V, 2.5 V, or 1.8 V
- Serial interface: I2C or SPI
- In-circuit programmable with non-volatile OTP memory
- ClockBuilder Pro software simplifies device configuration
- Si5341: 4 input, 10 output, 64-QFN 9x9 mm
- Si5340: 4 input, 4 output, 44-QFN 7x7 mm
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant

## 2. Ordering Guide

**Table 2.1. Si5341/40 Ordering Guide**

<table>
<tr><th>Ordering Part Number (OPN)</th><th>Number of Input/Output Clocks</th><th>Output Clock Frequency Range (MHz)</th><th>Frequency Synthesis Mode</th><th>Package</th><th>Temperature Range</th></tr>
<tr><td colspan="6">Si5341</td></tr>
<tr><td>Si5341A-D-GM[1, 2]</td><td rowspan="4">4/10</td><td>0.0001 to 1028 MHz</td><td rowspan="2">Integer and Fractional</td><td rowspan="4">64-QFN 9x9 mm</td><td rowspan="4">–40 to 85 °C</td></tr>
<tr><td>Si5341B-D-GM[1, 2]</td><td>0.0001 to 350 MHz</td></tr>
<tr><td>Si5341C-D-GM[1, 2]</td><td>0.0001 to 1028 MHz</td><td rowspan="2">Integer Only</td></tr>
<tr><td>Si5341D-D-GM[1, 2]</td><td>0.0001 to 350 MHz</td></tr>
<tr><td colspan="6">Si5340</td></tr>
<tr><td>Si5340A-D-GM[1, 2]</td><td rowspan="4">4/4</td><td>0.0001 to 1028 MHz</td><td rowspan="2">Integer and Fractional</td><td rowspan="4">44-QFN 7x7 mm</td><td rowspan="4">–40 to 85 °C</td></tr>
<tr><td>Si5340B-D-GM[1, 2]</td><td>0.0001 to 350 MHz</td></tr>
<tr><td>Si5340C-D-GM[1, 2]</td><td>0.0001 to 1028 MHz</td><td rowspan="2">Integer Only</td></tr>
<tr><td>Si5340D-D-GM[1, 2]</td><td>0.0001 to 350 MHz</td></tr>
<tr><td colspan="6">Si5341/40-D-EVB</td></tr>
<tr><td>Si5341-D-EVB</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">Evaluation Board</td><td rowspan="2">—</td></tr>
<tr><td>Si5340-D-EVB</td></tr>
</table>

**Note:**

1. Add an R at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory pre-programmed devices are available. Ordering part numbers are assigned by Silicon Labs and the ClockBuilder Pro software utility. Custom part number format is: e.g., Si5341A-Dxxxxx-GM, where "xxxxx" is a unique numerical sequence representing the preprogrammed configuration.
3. See 3.9 Custom Factory Preprogrammed Devicesand 3.10 Enabling Features and/or Configuration Settings Not Available in ClockBuilder Pro for Factory Pre-Programmed Devices for important notes about specifying a preprogrammed device to use features or device register settings not yet available in CBPro.

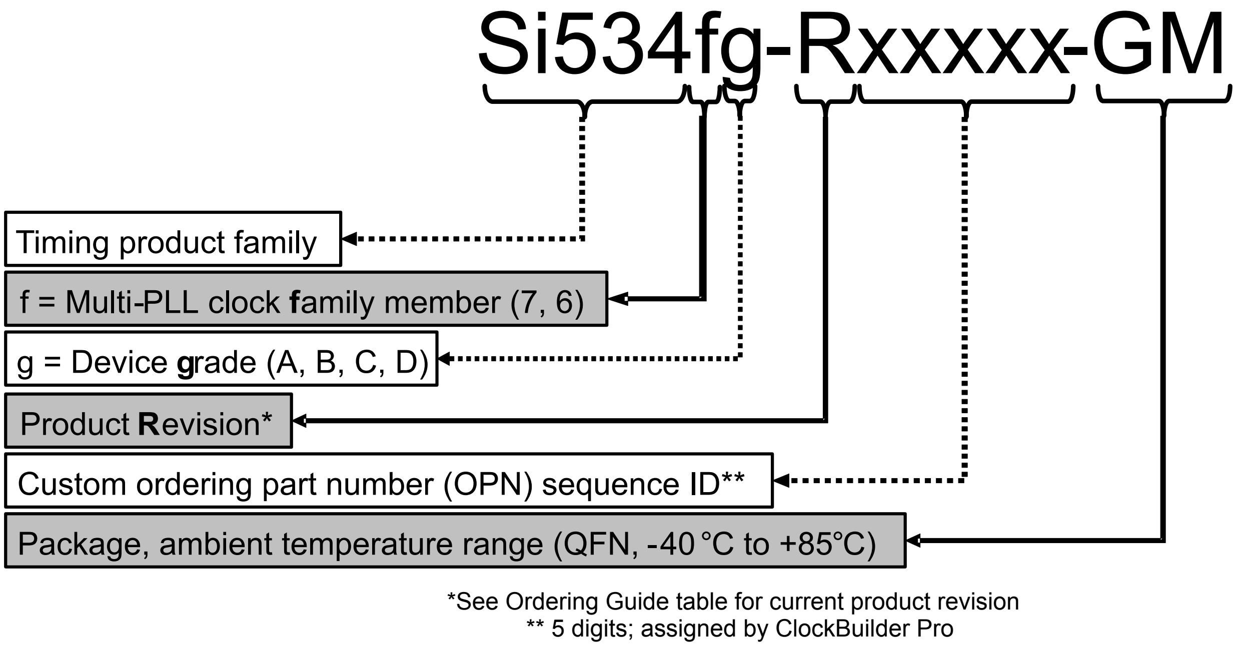



**Figure 2.1. Ordering Part Number Fields**

# 3. Functional Description

The Si5340/41-D combines a wide band PLL with next generation MultiSynth technology to offer the industry's most versatile and high performance clock generator. The PLL locks to either an external **crystal** between XA/XB or to an external **clock** connected to XA/XB or IN0, 1, 2. A fractional or integer multiplier takes the selected input clock or cystal frequency up to a very high frequency that is then divided by the MultiSynth output stage to any frequency in the range of 100 Hz to 1 GHz on each output. The MultiSynth stage can divide by both integer and fractional values. The high-resolution fractional MultiSynth dividers enable true any-frequency input to any-frequency on any of the outputs. The output drivers offer flexible output formats which are independently configurable on each of the outputs. This clock generator is fully configurable via its serial interface ($I^2C$/SPI) and includes in-circuit programmable non-volatile memory.

## 3.1 Power-up and Initialization

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is done. There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits will be restored to their initial state including the serial interface. A hard reset is initiated using the RSTb pin or by asserting the hard reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes.

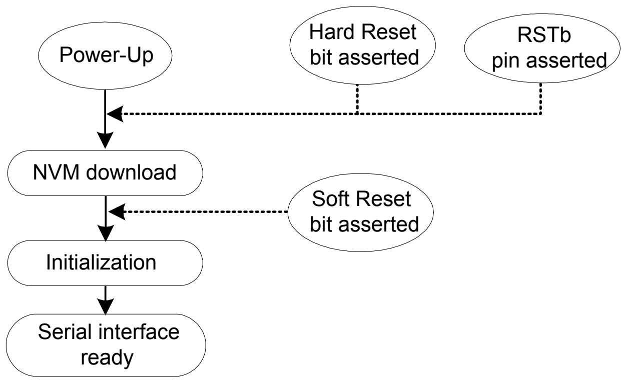



**Figure 3.1. Si5341 Power-Up and Initialization**

## 3.2 Frequency Configuration

The phase-locked loop is fully contained and does not require external loop filter components to operate. Its function is to phase lock to the selected input and provide a common reference to the MultiSynth high-performance fractional dividers.

A crosspoint mux connects any of the MultiSynth divided frequencies to any of the outputs drivers. Additional output integer dividers provide further frequency division by an even integer from 2 to (2^25)-2. The frequency configuration of the device is programmed by setting the input dividers (P), the PLL feedback fractional divider (Mn/Md), the MultiSynth fractional dividers (Nn/Nd), and the output integer dividers (R). Silicon Labs's ClockBuilder Pro configuration utility determines the optimum divider values for any desired input and output frequency plan.

## 3.3 Inputs

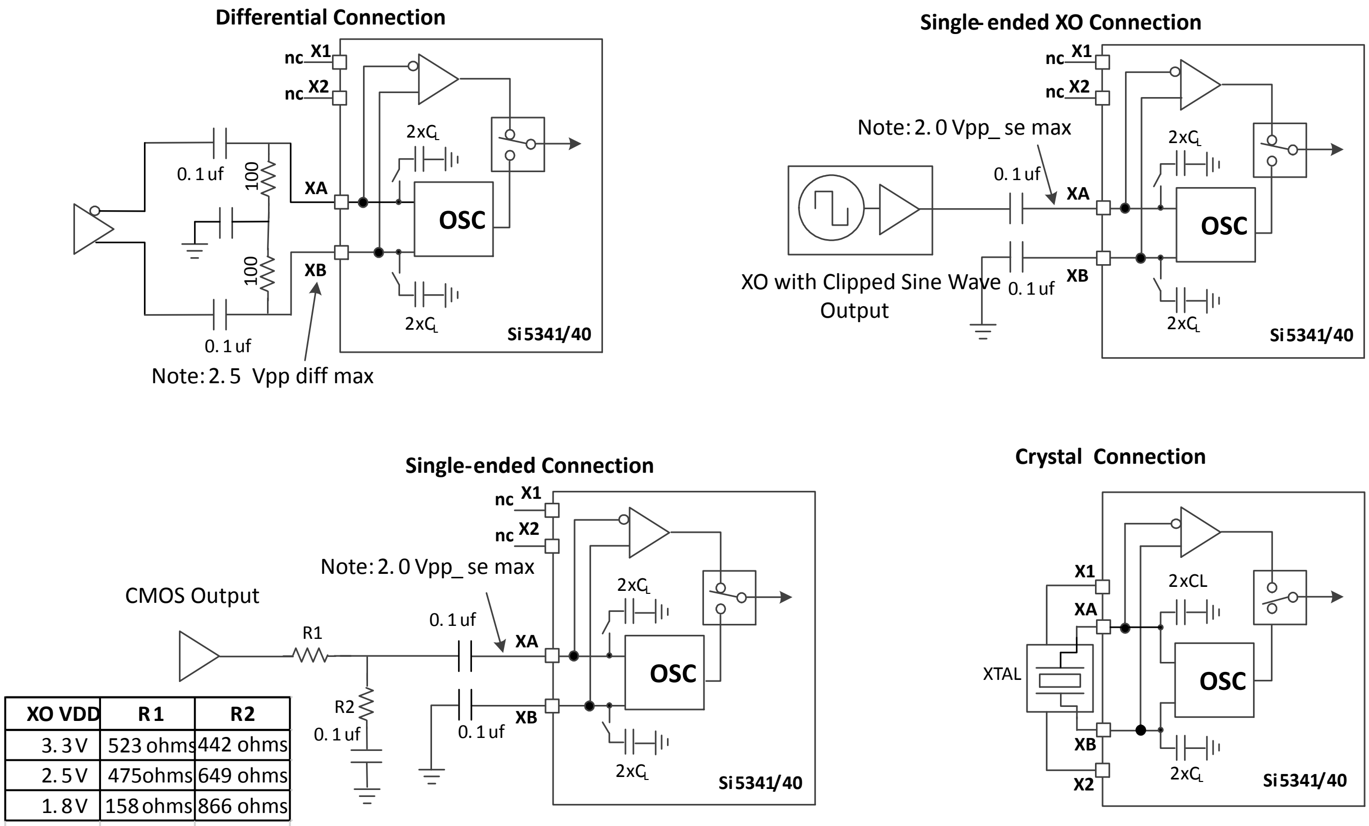
The Si5340/41-D requires either an external crystal at its XA/XB pins or an external clock at XA/XB or IN0, 1, 2.

### 3.3.1 XA/XB Clock and Crystal Input

An internal crystal oscillator exists between pin XA and XB. When this oscillator is enabled, an external crystal connected across these pins will oscillate and provide a clock input to the PLL. A crystal frequency of 25 MHz can be used although crystals in the frequency range of 48 MHz to 54 MHz are recommended for best jitter performance. Frequency offsets due to $C_L$ mismatch can be adjusted using the frequency adjustment feature which allows frequency adjustments of ± 1000 ppm. The Si5340/41 Family Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance. Refer to Table 5.12 Crystal Specifications on page 31 for crystal specifications.

To achieve optimal jitter performance and minimize BOM cost, a crystal is recommended on the XA/XB reference input. A clock (e.g., XO) may be used in lieu of the crystal, but it will result in higher output jitter. See the Si5340/41 Reference Manual for more information.

Selection between the external XTAL or input clock is controlled by register configuration. The internal crystal load capacitors ($C_L$) are disabled in the input clock mode. Refer to Table 5.3 Input Clock Specifications on page 20 for the input clock requirements at XAXB. Both a single-ended or a differential input clock can be connected to the XA/XB pins as shown in the figure below. A $P_{XAXB}$ divider is available to accommodate external clock frequencies higher than 54 MHz.

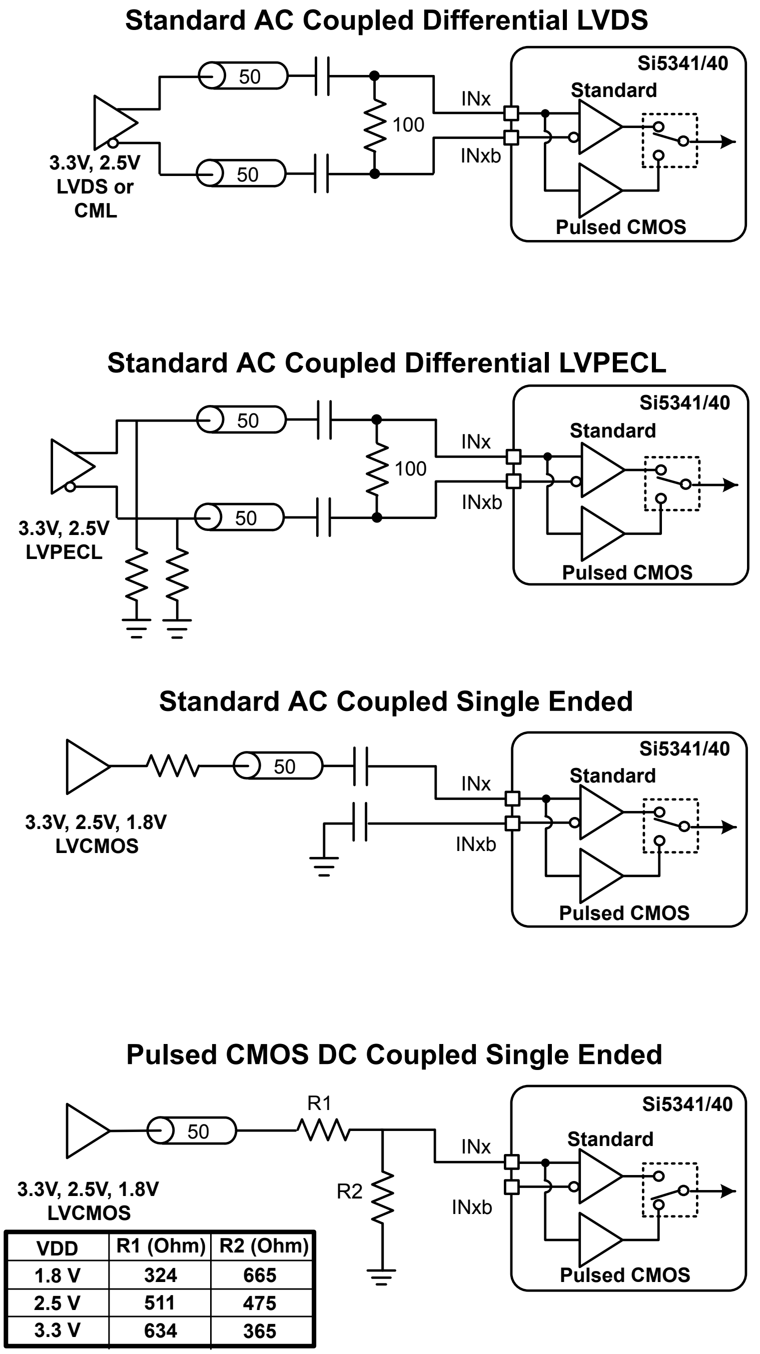



| XO VDD | R1 | R2 |
|---|---|---|
| 3.3 V | 523 ohms | 442 ohms |
| 2.5 V | 475ohms | 649 ohms |
| 1.8 V | 158 ohms | 866 ohms |

**Figure 3.2. XAXB External Crystal and Clock Connections**

### 3.3.2 Input Clocks (IN0, IN1, IN2)

A differential or single-ended clock can be applied at IN2, IN1, or IN0. The recommended input termination schemes are shown in the figure below.




| VDD | R1 (Ohm) | R2 (Ohm) |
|---|---|---|
| 1.8 V | 324 | 665 |
| 2.5 V | 511 | 475 |
| 3.3 V | 634 | 365 |

**Figure 3.3. Termination of Differential and LVCMOS Input Signals**

### 3.3.3 Input Selection (IN0, IN1, IN2, XA/XB)

The active clock input is selected using the IN_SEL[1:0] pins or by register control. A register bit determines input selection as pin or register selectable. There are internal pull ups on the IN_SEL pins.

**Table 3.1. Manual Input Selection Using IN_SEL[1:0] Pins**

| IN_SEL[1:0] | | Selected Input |
|---|---|---|
| 0 | 0 | IN0 |
| 0 | 1 | IN1 |
| 1 | 0 | IN2 |
| 1 | 1 | XA/XB |

## 3.4 Fault Monitoring

The Si5340/41-D provides fault indicators which monitor loss of signal (LOS) of the inputs (IN0, IN1, IN2, XA/XB, FB_IN) and loss of lock (LOL) for the PLL as shown in the figure below.

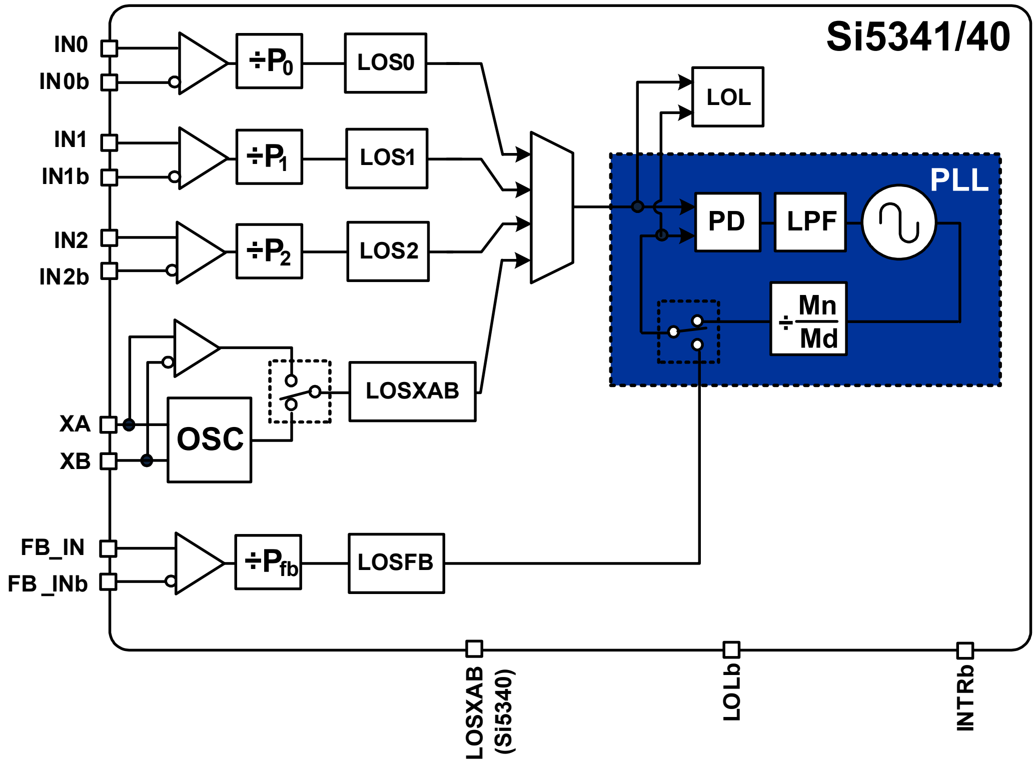



**Figure 3.4. LOS and LOL Fault Monitors**

### 3.4.1 Status Indicators

The state of the status monitors are accessible by reading registers through the serial interface or with dedicated pin (LOLb). Each of the status indicator register bits has a corresponding sticky bit in a separate register location. Once a status bit is asserted its corresponding sticky bit (_FLG) will remain asserted until cleared. Writing a logic zero to a sticky register bit clears its state.

### 3.4.2 Interrupt Pin (INTRb)

An interrupt pin (INTRb) indicates a change in state with any of the status registers. All status registers are maskable to prevent assertion of the interrupt pin. The state of the INTRb pin is reset by clearing the status registers.

### 3.5 Outputs

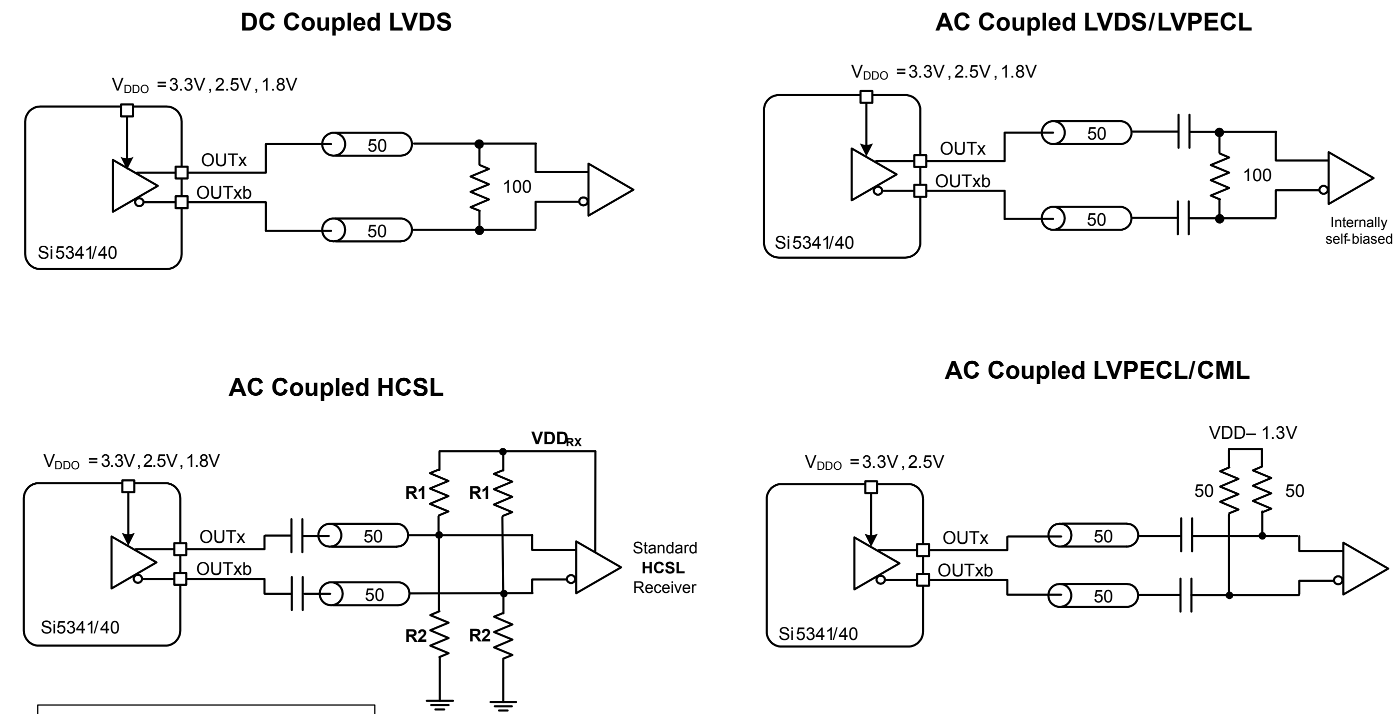
The Si5341 supports 10 differential output drivers which can be independently configured as differential or LVCMOS. The Si5340 supports 4 output drivers independently configurable as differential or LVCMOS.

#### 3.5.1 Output Signal Format

The differential output amplitude and common mode voltage are both fully programmable and compatible with a wide variety of signal formats including LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 20 single-ended outputs, or any combination of differential and single-ended outputs.

#### 3.5.2 Differential Output Terminations

The differential output drivers support both ac-coupled and dc-coupled terminations as shown in the figure below.




| For $V_{CM}$ = 0.37V | | |
|---|---|---|
| $VDD_{RX}$ | R1 | R2 |
| 3.3V | 442 ohms | 56.2 ohms |
| 2.5V | 332 ohms | 59 ohms |
| 1.8V | 243 ohms | 63.4 ohms |

**Figure 3.5. Supported Differential Output Terminations**

#### 3.5.3 Programmable Common Mode Voltage for Differential Outputs

The common mode voltage (VCM) for the differential modes are programmable so that LVDS specifications can be met and for the best signal integrity with different supply voltages. When dc coupling the output driver it is essential that the receiver should have a relatively high common mode impedance so that the common mode current from the output driver is very small.

### 3.5.4 LVCMOS Output Terminations

LVCMOS outputs are typically dc-coupled, as shown in the figure below.

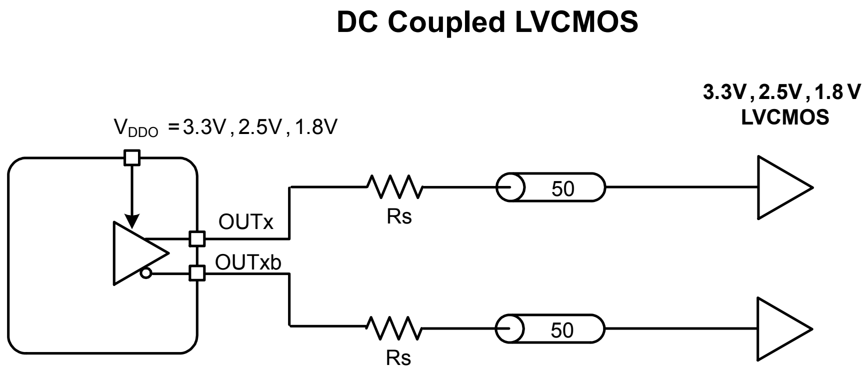



**Figure 3.6. LVCMOS Output Terminations**

### 3.5.5 LVCMOS Output Impedance and Drive Strength Selection

Each LVCMOS driver has a configurable output impedance. It is highly recommended that the minimum output impedance (strongest drive setting) is selected and a suitable series resistor (Rs) is chosen to match the trace impedance.

**Table 3.2. Nominal Output Impedance vs. OUTx_CMOS_DRV (register)**

| VDDO | CMOS_DRIVE_Selection | | |
|---|---|---|---|
| | OUTx_CMOS_DRV=1 | OUTx_CMOS_DRV=2 | OUTx_CMOS_DRV=3 |
| 3.3 V | 38 Ω | 30 Ω | 22 Ω |
| 2.5 V | 43 Ω | 35 Ω | 24 Ω |
| 1.8 V | — | 46 Ω | 31 Ω |
| **Note:** Refer to the Si5340/41 Family Reference Manual for more information on register settings. | | | |

### 3.5.6 LVCMOS Output Signal Swing

The signal swing ($V_{OL}$/$V_{OH}$) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers.

### 3.5.7 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUTx and OUTxb). By default the clock on the OUTxb pin is generated with complementary polarity with the clock on the OUTx pin. The LVCMOS OUTx and OUTxb outputs can also be generated in phase.

### 3.5.8 Output Enable/Disable

The OEb pin provides a convenient method of disabling or enabling the output drivers. When the OEb pin is held high all outputs will be disabled. When held low, the outputs will be enabled. Outputs in the enabled state can be individually disabled through register control.

### 3.5.9 Output Driver State When Disabled

The disabled state of an output driver is configurable as: disable low or disable high.

### 3.5.10 Synchronous/Asynchronous Output Disable Feature

Outputs can be configured to disable synchronously or asynchronously. The default state is synchronous output disable. In synchronous disable mode the output will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. In asynchronous disable mode the output clock will disable immediately without waiting for the period to complete.

### 3.5.11 Output Delay Control ($t_0$-$t_4$)

The Si5341/40 uses independent MultiSynth dividers ($N_0$ - $N_4$) to generate up to 5 unique frequencies to its 10 outputs through a cross-point switch. By default all clocks are phase aligned. A delay path (t0 - t4) associated with each of these dividers is available for applications that need a specific output skew configuration. Each delay path is controlled by a register parameter call Nx_DELAY with a resolution of ~0.28 ps over a range of ~±9.14 ns. This is useful for PCB trace length mismatch compensation. After the delay controls are configured, the soft reset bit SOFT_RST must be set high so that the output delay takes effect and the outputs are re-aligned.

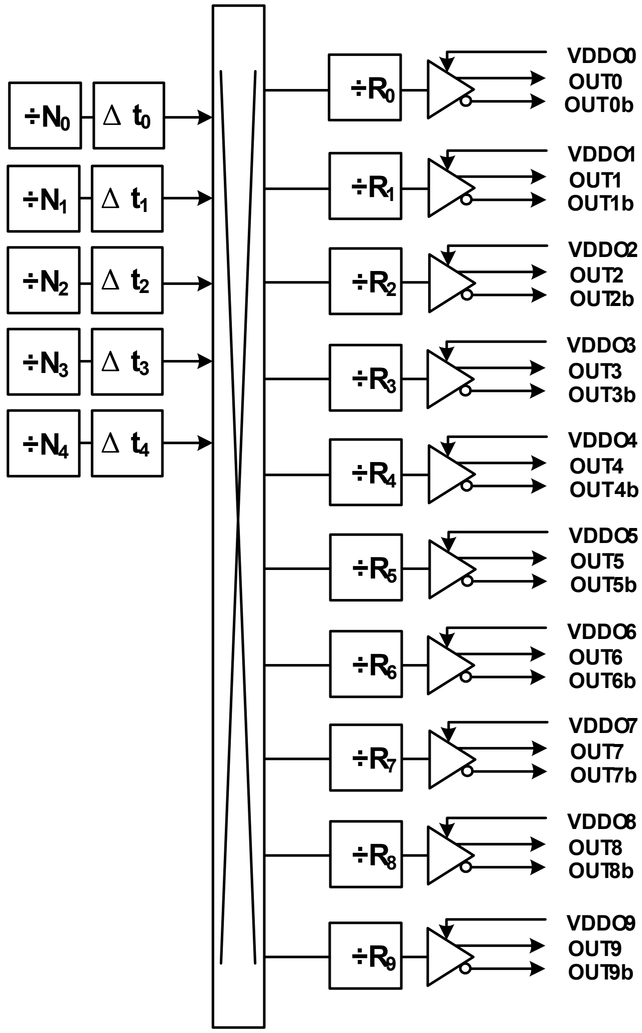



**Figure 3.7. Example of Independently Configurable Path Delays**

All delay values are restored to their NVM programmed values after power-up or after a hard reset. Delay default values can be written to the NVM allowing a custom delay offset configuration at power-up or after a hardware reset.

### 3.5.12 Zero Delay Mode

A zero delay mode is available for applications that require fixed and consistent minimum delay between the selected input and outputs. The zero delay mode is configured by opening the internal feedback loop through software configuration and closing the loop externally as shown in the figure below. This helps to cancel out the internal delay introduced by the dividers, the crosspoint, the input, and the output drivers. Any one of the outputs can be fed back to the FB_IN pins, although using the output driver that achieves the shortest trace length will help to minimize the input-to-output delay. It is recommended to connect OUT9 (Si5341) or OUT3 (Si5340) to FB_IN for external feedback. The FB_IN input pins must be terminated and ac-coupled when zero delay mode is used. A differential external feedback path connection is necessary for best performance.

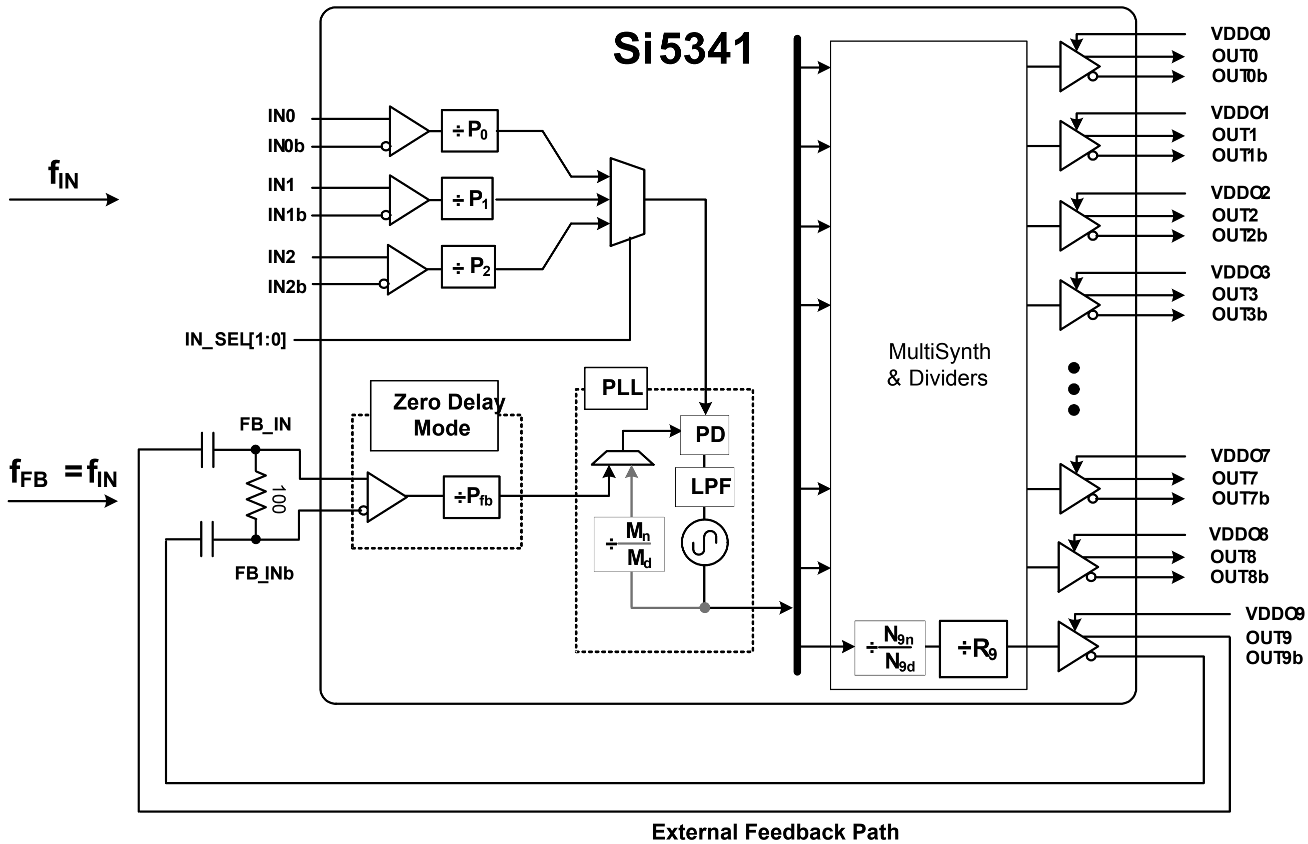



**Figure 3.8. Si5341 Zero Delay Mode Setup**

### 3.5.13 Sync Pin (Synchronizing R Dividers)

All the output R dividers are reset to the default NVM register state after a power-up or a hard reset. This ensures consistent and repeatable phase alignment across all output drivers to within ±100 ps of the expected value from the NVM download. Resetting the device using the RSTb pin or asserting the hard reset bit will have the same result. The SYNCb pin provides another method of re-aligning the R dividers without resetting the device, however, the outputs will only align to within 50 ns when using the SYNCb pin. This pin is positive edge triggered. Asserting the sync register bit provides the same function as the SYNCb pin. A soft reset will align the outputs to within ±100 ps of the expected value based upon the Nx_DELAY parameter.

### 3.5.14 Output Crosspoint

The output crosspoint allows any of the N dividers to connect to any of the clock outputs.

#### 3.5.15 Digitally Controlled Oscillator (DCO) Modes

Each MultiSynth can be digitally controlled so that all outputs connected to the MultiSynth change frequency in real time without any transition glitches. There are two ways to control the MultiSynth to accomplish this task:

- Use the Frequency Increment/Decrement Pins or register bits.
- Write directly to the numerator of the MultiSynth divider.

An output that is controlled as a DCO is useful for simple tasks such as frequency margining or CPU speed control. The output can also be used for more sophisticated tasks such as FIFO management by adjusting the frequency of the read or write clock to the FIFO or using the output as a variable Local Oscillator in a radio application.

##### 3.5.15.1 DCO with Frequency Increment/Decrement Pins/Bits

Each of the MultiSynth fractional dividers can be independently stepped up or down in predefined steps with a resolution as low as 0.001 ppb. Setting of the step size and control of the frequency increment or decrement is accomplished by setting the step size with the 44 bit Frequency Step Word (FSTEPW). When the FINC or FDEC pin or register bit is asserted the output frequency will increment or decrement respectively by the amount specified in the FSTEPW.

##### 3.5.15.2 DCO with Direct Register Writes

When a MultiSynth numerator and its corresponding update bit is written, the new numerator value will take effect and the output frequency will change without any glitches. The MultiSynth numerator and denominator terms can be left and right shifted so that the least significant bit of the numerator word represents the exact step resolution that is needed for your application.

### 3.6 Power Management

Several unused functions can be powered down to minimize power consumption. Consult the Si5340/41 Family Reference Manual and ClockBuilder Pro configuration utility for details.

### 3.7 In-Circuit Programming

The Si5341/40 is fully configurable using the serial interface ($I^2C$ or SPI). At power-up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its $V_{DD}$ and $V_{DDA}$ pins. The NVM is two time writable. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Refer to the Si5340/41 Family Reference Manual for a detailed procedure for writing registers to NVM.

### 3.8 Serial Interface

Configuration and operation of the Si5341/40 is controlled by reading and writing registers using the $I^2C$ or SPI interface. The I2C_SEL pin selects $I^2C$ or SPI operation. Communication with both 3.3 V and 1.8 V host is supported. The SPI mode operates in either 4-wire or 3-wire. See the Si5340/41 Family Reference Manual for details.

### 3.9 Custom Factory Preprogrammed Devices

For applications where a serial interface is not available for programming the device, custom pre-programmed parts can be ordered with a specific configuration written into NVM. A factory pre-programmed device will generate clocks at power-up. Custom, factory-preprogrammed devices are available. Use the ClockBuilder Pro custom part number wizard (www.silabs.com/clockbuilderpro) to quickly and easily request and generate a custom part number for your configuration. In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Silicon Labs sales representative. Samples of your pre-programmed device will ship to you typically within two weeks.

### 3.10 Enabling Features and/or Configuration Settings Not Available in ClockBuilder Pro for Factory Pre-Programmed Devices

As with essentially all software utilities, ClockBuilder Pro is continuously updated and enhanced. By registering at http://www.silabs.comand opting in for updates to software, you will be notified whenever changes are made and what the impact of those changes are. This update process will ultimately enable ClockBuilder Pro users to access all features and register setting values documented in this data sheet and the Si5341/40 Family Reference Manual. However, if you must enable or access a feature or register setting value so that the device starts up with this feature or a register setting, but the feature or register setting is NOT yet available in CBPro, you must contact a Silicon Labs applications engineer for assistance. An example of this type of feature or custom setting is the customizable amplitudes for the clock outputs. After careful review of your project file and custom requirements, a Silicon Labs applications engineer will email back your CBPro project file with your specific features and register settings enabled, using what is referred to as the manual "settings override" feature of CBPro. "Override" settings to match your request(s) will be listed in your design report file. Examples of setting "overrides" in a CBPro design report are shown below:

**Table 3.3. Setting Overrides**

| Location | Name | Type | Target | Dec Value | Hex Value |
|---|---|---|---|---|---|
| 0128[6:4] | OUT6_AMPL | User | OPN & EVB | 5 | 5 |

Once you receive the updated design file, simply open it in CBPro. After you create a custom OPN, the device will begin operation after startup with the values in the NVM file, including the Silicon Labs-supplied override settings.

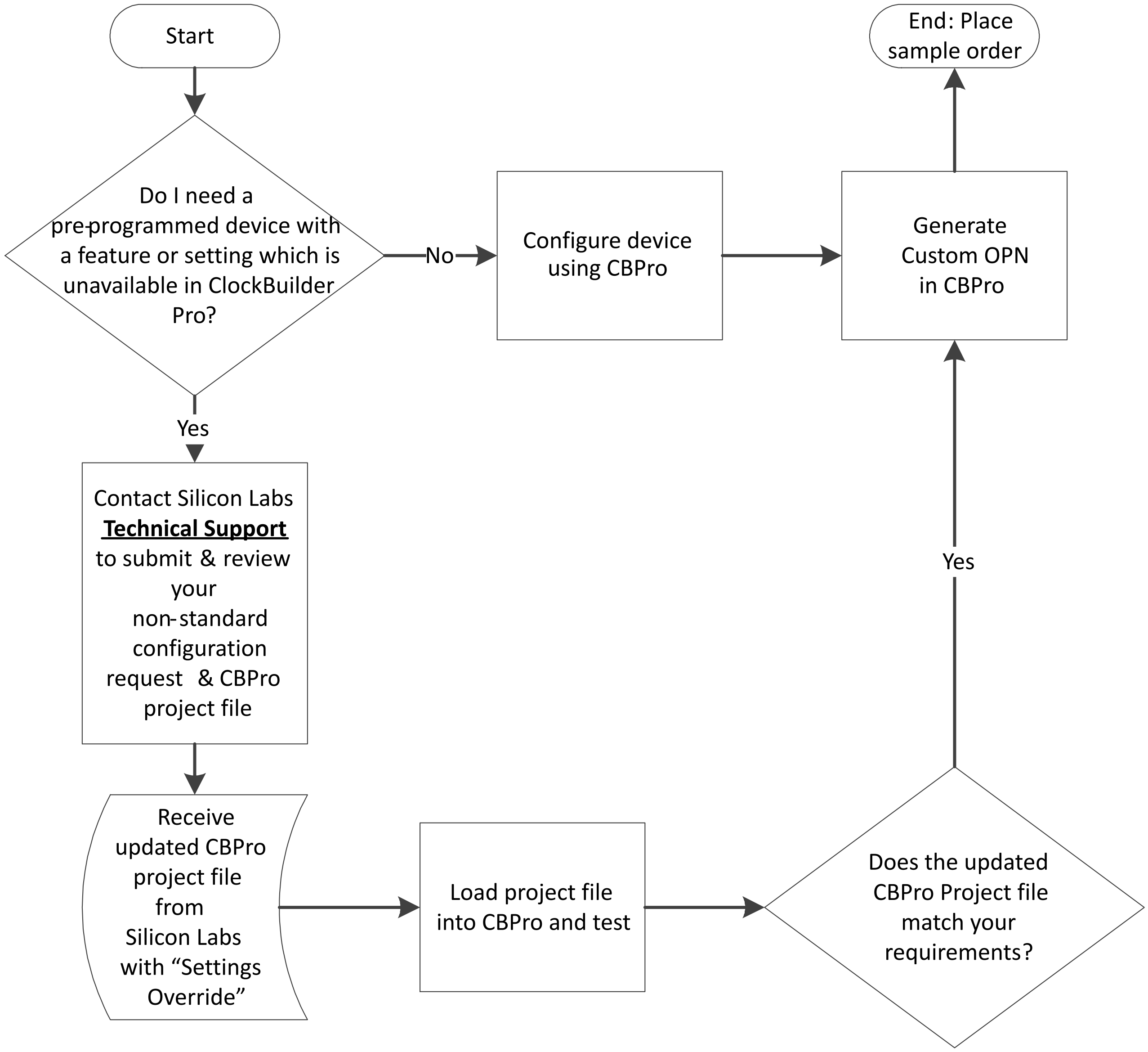



**Figure 3.9. Flowchart to Order Custom Parts with Features not Available in CBPro**

**Note:** Contact Silicon Labs Technical Support at www.silabs.com/support/Pages/default.aspx.

# 4. Register Map

The register map is divided into multiple pages where each page has 256 addressable registers. Page 0 contains frequently accessible registers such as alarm status, resets, device identification, etc. Other pages contain registers that need less frequent access such as frequency configuration, and general device settings. A high level map of the registers is shown in 4.2 High-Level Register Map. Refer to the Si5340/41 Family Reference Manual for a complete list of register descriptions and settings.

## 4.1 Addressing Scheme

The device registers are accessible using a 16-bit address which consists of an 8-bit page address + 8-bit register address. By default the page address is set to 0x00. Changing to another page is accomplished by writing to the 'Set Page Address' byte located at address 0x01 of each page.

## 4.2 High-Level Register Map

**Table 4.1. High-Level Register Map**

| 16-Bit Address | | Content |
|---|---|---|
| 8-bit Page Address | 8-bit Register Address Range | |
| 00 | 00 | Revision IDs |
| | 01 | Set Page Address |
| | 02-0A | Device IDs |
| | 0B-15 | Alarm Status |
| | 17-1B | INTR Masks |
| | 1C | Reset controls |
| | 2C-E1 | Alarm Configuration |
| | E2-E4 | NVM Controls |
| | FE | Device Ready Status |
| 01 | 01 | Set Page Address |
| | 08-3A | Output Driver Controls |
| | 41-42 | Output Driver Disable Masks |
| | FE | Device Ready Status |
| 02 | 01 | Set Page Address |
| | 02-05 | XTAL Frequency Adjust |
| | 08-2F | Input Divider (P) Settings |
| | 30 | Input Divider (P) Update Bits |
| | 35-3D | PLL Feedback Divider (M) Settings |
| | 3E | PLL Feedback Divider (M) Update Bit |
| | 47-6A | Output Divider (R) Settings |
| | 6B-72 | User Scratch Pad Memory |
| | FE | Device Ready Status |
| 03 | 01 | Set Page Address |
| | 02-37 | MultiSynth Divider (N0-N4) Settings |
| | 0C | MultiSynth Divider (N0) Update Bit |
| | 17 | MultiSynth Divider (N1) Update Bit |
| | 22 | MultiSynth Divider (N2) Update Bit |
| | 2D | MultiSynth Divider (N3) Update Bit |
| | 38 | MultiSynth Divider (N4) Update Bit |
| | 39-58 | FINC/FDEC Settings N0-N4 |
| | 59-62 | Output Delay (Dt) Settings |
| | 63-94 | Frequency Readback N0-N4 |
| | FE | Device Ready Status |

| 16-Bit Address | | Content |
|---|---|---|
| 8-bit Page Address | 8-bit Register Address Range | |
| 04-08 | 00-FF | Reserved |
| 09 | 01 | Set Page Address |
| | 49 | Input Settings |
| | 1C | Zero Delay Mode Settings |
| A0-FF | 00-FF | Reserved |

# 5. Electrical Specifications

**Table 5.1. Recommended Operating Conditions[1]**

($V_{DD}$=1.8 V ± 5%, $V_{DDA}$=3.3 V ± 5%, $T_A$= –40 to 85°C)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Ambient Temperature | $T_A$ | –40 | 25 | 85 | °C |
| Junction Temperature | $TJ_{MAX}$ | — | — | 125 | °C |
| Core Supply Voltage | $V_{DD}$ | 1.71 | 1.80 | 1.89 | V |
| | $V_{DDA}$ | 3.14 | 3.30 | 3.47 | V |
| Output Driver Supply Voltage | $V_{DDO}$ | 3.14 | 3.30 | 3.47 | V |
| | | 2.37 | 2.50 | 2.62 | V |
| | | 1.71 | 1.80 | 1.89 | V |

**Note:**

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

**Table 5.2. DC Characteristics**

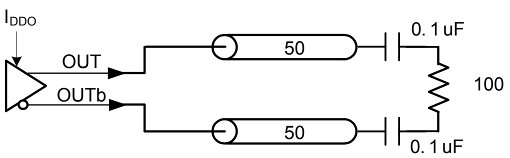
($V_{DD}$=1.8V ± 5%, $V_{DDA}$=3.3V ± 5%, $V_{DDO}$=1.8V ± 5%, 2.5V ± 5%, or 3.3V ± 5%, $T_A$= -40 to 85°C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Core Supply Current[1, 2] | $I_{DD}$ | Si5340/41 | — | 115 | 230 | mA |
| | $I_{DDA}$ | Si5340/41 | — | 120 | 130 | mA |
| Output Buffer Supply Current | $I_{DDOx}$ | LVPECL Output[3] @ 156.25 MHz | — | 22 | 26 | mA |
| | | LVDS Output[3] @ 156.25 MHz | — | 15 | 18 | mA |
| | | 3.3 V LVCMOS[4] output @ 156.25 MHz | — | 22 | 30 | mA |
| | | 2.5 V LVCMOS[4] output @ 156.25 MHz | — | 18 | 23 | mA |
| | | 1.8 V LVCMOS[4] output @ 156.25 MHz | — | 12 | 16 | mA |
| Total Power Dissipation[1, 5] | $P_d$ | Si5341 | — | 880 | 1150 | mW |
| | | Si5340 | — | 680 | 875 | mW |

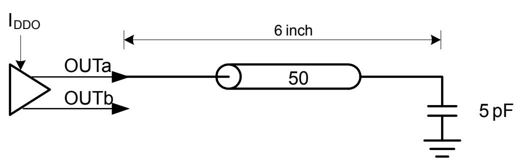
**Note:**

1. Si5341 test configuration: 7 x 2.5 V LVDS outputs enabled @ 156.25 MHz. Excludes power in termination resistors.
2. Si5340 test configuration: 4 x 2.5 V LVDS outputs enabled @ 156.25 MHz. Excludes power in termination resistors.
3. Differential outputs terminated into an ac-coupled 100 Ω load.
4. LVCMOS outputs measured into a 6-inch 50 W PCB trace with 5 pF load. The LVCMOS outputs were set to OUTx_CMOS_DRV=3, which is the strongest driver setting. Refer to the Si5341/40 Family Reference Manual for more details on register settings.

**Differential Output Test Configuration**




**LVCMOS Output Test Configuration**




5. Detailed power consumption for any configuration can be estimated using ClockBuilderPro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

**Table 5.3. Input Clock Specifications**

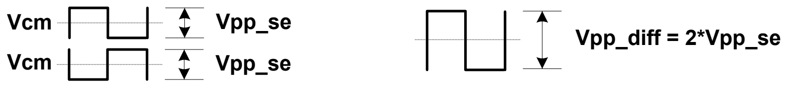
($V_{DD}$=1.8V ± 5%, $V_{DDA}$=3.3V ± 5%, $T_A$=-40 to 85°C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Standard Input Buffer with Differential or Single-Ended - AC-Coupled (IN0/IN0b, IN1/IN1b, IN2/IN2b, FB_IN/FB_INb)** | | | | | | |
| Input Frequency Range | $f_{IN}$ | Differential | 0.008 | — | 750 | MHz |
| | | All Single-ended Signals (including LVCMOS) | 0.008 | — | 250 | MHz |
| Input Voltage Swing[1] | $V_{IN}$ | Differential AC-coupled $f_{IN}$ < 250 MHz | 100 | — | 1800 | mVpp_se |
| | | Differential AC-coupled 250 MHz < $f_{IN}$ < 750 MHz | 225 | — | 1800 | mVpp_se |
| | | Single-ended AC-coupled $f_{IN}$ < 250 MHz | 100 | — | 3600 | mVpp_se |
| Slew Rate[2, 3] | SR | | 400 | — | — | V/µs |
| Duty Cycle | DC | | 40 | — | 60 | % |
| Input Capacitance | $C_{IN}$ | | — | 0.3 | — | pF |
| Input Resistance | $R_{IN}$ | | — | 16 | — | kΩ |
| **Pulsed CMOS Input Buffer - DC Coupled (IN0, IN1, IN2)[4]** | | | | | | |
| Input Frequency | $f_{IN}$ | | 0.008 | — | 250 | MHz |
| Input Voltage | $V_{IL}$ | | –0.2 | — | 0.4 | V |
| | $V_{IH}$ | | 0.8 | — | — | V |
| Slew Rate[2, 3] | SR | | 400 | — | — | V/µs |
| Duty Cycle | DC | Clock Input | 40 | — | 60 | % |
| Minimum Pulse Width | PW | Pulse Input | 1.6 | — | — | ns |
| Input Resistance | $R_{IN}$ | | — | 8 | — | kΩ |
| **REFCLK (Applied to XA/XB)** | | | | | | |
| Input Frequency Range | $f_{IN}$ | Full operating range. Jitter performance may be reduced. | 10 | — | 200 | MHz |
| | | Range for best jitter. | 48 | — | 54 | MHz |
| Input Single-ended Voltage Swing | $V_{IN\_SE}$ | | 365 | — | 2000 | mVpp_se |
| Input Differential Voltage Swing | $V_{IN\_DIFF}$ | | 365 | — | 2500 | mVpp_diff |
| Slew Rate[2, 3] | SR | Imposed for best jitter performance | 400 | — | — | V/µs |
| Input Duty Cycle | DC | | 40 | — | 60 | % |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|

**Note:**

1. Voltage swing is specified as single-ended mVpp.




2. Imposed for jitter performance.
3. Pulsed CMOS mode is intended primarily for single-ended LVCMOS input clocks < 1 MHz, which must be dc-coupled because they have a duty cycle significantly less than 50%. A typical application example is a low frequency video frame sync pulse. Since the input thresholds ($V_{IL}$, $V_{IH}$) of this buffer are non-standard (0.4 and 0.8 V, respectively), refer to the input attenuator circuit for DC-coupled Pulsed LVCMOS in the Family Reference Manual. Otherwise, for standard LVCMOS input clocks, use the Standard AC-Coupled, Single-ended input mode.
4. DC-coupled CMOS Input Buffer selection is not supported in ClockBuilder Pro for new designs. For single-ended LVCMOS inputs to IN0,1,2 it is required to ac-couple into the differential input buffer.

**Table 5.4. Control Input Pin Specifications**

($V_{DD}$=1.8V ± 5%, $V_{DDA}$=3.3V ± 5%, $V_{DDS}$=3.3V ± 5%, 1.8V ± 5%, $T_A$=-40 to 85°C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Si5341 Control Input Pins (I2C_SEL, IN_SEL[1:0], RSTb, OEb, SYNCb, A1, SCLK, A0/CSb, FINC, FDEC, SDA/SDIO)** | | | | | | |
| Input Voltage | $V_{IL}$ | | — | — | $0.3xV_{DDIO}$[1] | V |
| | $V_{IH}$ | | $0.7xV_{DDIO}$[1] | — | — | V |
| Input Capacitance | $C_{IN}$ | | — | 2 | — | pF |
| Input Resistance | $R_{IN}$ | | — | 20 | — | kW |
| Minimum Pulse Width | $T_{PW}$ | RSTb, SYNCb, FINC, and FDEC | 100 | — | — | ns |
| Frequency Update Rate | $F_{UR}$ | FINC and FDEC | — | — | 1 | MHz |
| **Si5340 Control Input Pins (I2C_SEL, IN_SEL[1:0], RSTb, OEb, A1, SCLK, A0/CSb, SDA/SDIO)** | | | | | | |
| Input Voltage | $V_{IL}$ | | — | — | $0.3xV_{DDIO}$[1] | V |
| | $V_{IH}$ | | $0.7xV_{DDIO}$[1] | — | — | V |
| Input Capacitance | $C_{IN}$ | | — | 2 | — | pF |
| Input Resistance | $R_{IN}$ | | — | 20 | — | kW |
| Minimum Pulse Width | $T_{PW}$ | RSTb only | 100 | — | — | ns |

**Note:**

1. $V_{DDIO}$ is determined by the IO_VDD_SEL bit. It is selectable as $V_{DDA}$ or $V_{DD}$. Refer to the Family Reference Manual for more details on register settings.

**Table 5.5. Differential Clock Output Specifications**

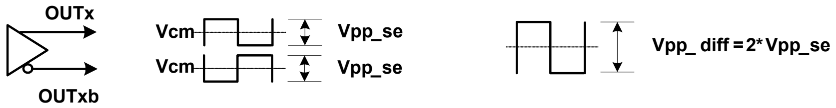
($V_{DD}$=1.8 V ± 5%, $V_{DDA}$=3.3V ± 5%, $V_{DDO}$=1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 5%, $T_A$= -40 to 85°C)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Output Frequency | $f_{OUT}$ | MultiSynth not used | | 0.0001 | — | 720 | MHz |
| | | | | 733.33 | — | 800.00 | |
| | | | | 825 | — | 1028 | |
| | | MultiSynth used | | 0.0001 | — | 720 | MHz |
| Duty Cycle | DC | $f_{OUT}$ < 400 MHz | | 48 | — | 52 | % |
| | | 400 MHz < $f_{OUT}$ < 1028 MHz | | 45 | — | 55 | % |
| Output-Output Skew<br>Using Same MultiSynth | $T_{SKS}$ | Outputs on same MultiSynth<br>(Measured at 712.5 MHz) | | — | — | 65 | ps |
| Output-Output Skew<br>Between MultiSynths | $T_{SKD}$ | Outputs from different MultiSynths<br>(Measured at 712.5 MHz) | | — | — | 90 | ps |
| OUT-OUTb Skew | $T_{SK\_OUT}$ | Measured from the positive to negative output pins | | — | 0 | 50 | ps |
| Output Voltage Swing[1] | $V_{OUT}$ | LVDS | | 350 | 430 | 510 | mVpp_se |
| | | LVPECL | | 640 | 750 | 900 | |
| Common Mode Voltage[1, 2] | $V_{CM}$ | $V_{DDO}$ = 3.3 V | LVDS | 1.10 | 1.2 | 1.3 | V |
| | | | LVPECL | 1.90 | 2.0 | 2.1 | |
| | | $V_{DDO}$ = 2.5 V | LVPECL<br>LVDS | 1.1 | 1.2 | 1.3 | |
| | | $V_{DDO}$ = 1.8 V | Sub-LVDS | 0.8 | 0.9 | 1.0 | |
| Rise and Fall Times<br>(20% to 80%) | $t_R/t_F$ | | | — | 100 | 150 | ps |
| Differential Output Impedance | $Z_O$ | | | — | 100 | — | Ω |
| Power Supply Noise Rejection[2] | PSRR | 10 kHz sinusoidal noise | | — | –101 | — | dBc |
| | | 100 kHz sinusoidal noise | | — | –96 | — | |
| | | 500 kHz sinusoidal noise | | — | –99 | — | |
| | | 1 MHz sinusoidal noise | | — | –97 | — | |
| Output-Output Crosstalk[3] | XTALK | Si5341 | | — | –72 | — | dBc |
| | | Si5340 | | — | –88 | — | dBc |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|

**Notes:**

1. Output amplitude and common-mode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The maximum LVDS single-ended amplitude can be up to 110 mV higher than the TIA/EIA-644 maximum. Refer to the Si5341/40 Family Reference Manual for more suggested output settings. Not all combinations of voltage amplitude and common mode voltages settings are possible.




2. Measured for 156.25 MHz carrier frequency. 100 mVpp sinewave noise added to VDDO = 3.3 V and noise spur amplitude measured.
3. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to application note, AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems, guidance on crosstalk minimization.

**Table 5.6. LVCMOS Clock Output Specifications**

($V_{DD}$=1.8V ± 5%, $V_{DDA}$=3.3V ± 5%, $V_{DDO}$=1.8V ± 5%, 2.5V ± 5%, or 3.3V ± 5%, $T_A$= -40 to 85°C)

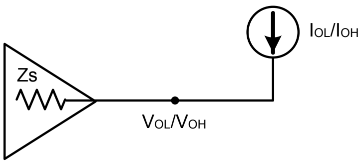
| Parameter | Symbol | Test Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Output Frequency | | | | 0.0001 | — | 250 | MHz |
| Duty Cycle | DC | $f_{OUT}$ < 100 MHz | | 48 | — | 52 | % |
| | | 100 MHz < $f_{OUT}$ < 250 MHz | | 45 | — | 55 | |
| Output-to-Output Skew | $T_{SK}$ | Outputs on same MultiSynth. $F_{OUT}$ = 156.25 MHz | | — | 30 | 140 | ps |
| Output Voltage High[1, 2, 3] | $V_{OH}$ | $V_{DDO}$ = 3.3 V | | | | | |
| | | OUTx_CMOS_DRV=1 | $I_{OH}$ = -10 mA | $V_{DDO}$ x 0.85 | — | — | V |
| | | OUTx_CMOS_DRV=2 | $I_{OH}$ = -12 mA | | — | — | |
| | | OUTx_CMOS_DRV=3 | $I_{OH}$ = -17 mA | | — | — | |
| | | $V_{DDO}$ = 2.5 V | | | | | |
| | | OUTx_CMOS_DRV=1 | $I_{OH}$ = -6 mA | $V_{DDO}$ x 0.85 | — | — | V |
| | | OUTx_CMOS_DRV=2 | $I_{OH}$ = -8 mA | | — | — | |
| | | OUTx_CMOS_DRV=3 | $I_{OH}$ = -11 mA | | — | — | |
| | | $V_{DDO}$ = 1.8 V | | | | | |
| | | OUTx_CMOS_DRV=2 | $I_{OH}$ = -4 mA | $V_{DDO}$ x 0.85 | — | — | V |
| | | OUTx_CMOS_DRV=3 | $I_{OH}$ = -5 mA | | — | — | |

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Output Voltage Low[1, 2, 3] | $V_{OL}$ | $V_{DDO}$ = 3.3 V | | | | | |
| | | OUTx_CMOS_DRV=1 | $I_{OL}$ = 10 mA | — | — | $V_{DDO}$ x 0.15 | V |
| | | OUTx_CMOS_DRV=2 | $I_{OL}$ = 12 mA | — | — | | |
| | | OUTx_CMOS_DRV=3 | $I_{OL}$ = 17 mA | — | — | | |
| | | $V_{DDO}$ = 2.5 V | | | | | |
| | | OUTx_CMOS_DRV=1 | $I_{OL}$ = 6 mA | — | — | $V_{DDO}$ x 0.15 | V |
| | | OUTx_CMOS_DRV=2 | $I_{OL}$ = 8 mA | — | — | | |
| | | OUTx_CMOS_DRV=3 | $I_{OL}$ = 11 mA | — | — | | |
| | | $V_{DDO}$ = 1.8 V | | | | | |
| | | OUTx_CMOS_DRV=2 | $I_{OL}$ = 4 mA | — | — | $V_{DDO}$ x 0.15 | V |
| | | OUTx_CMOS_DRV=3 | $I_{OL}$ = 5 mA | — | — | | |
| LVCMOS Rise and Fall Times[3]<br>(20% to 80%) | tr/tf | VDDO = 3.3V | | — | 400 | 600 | ps |
| | | VDDO = 2.5 V | | — | 450 | 600 | ps |
| | | VDDO = 1.8 V | | — | 550 | 750 | ps |

**Notes:**

1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Family Reference Manual for more details on register settings.
2. $I_{OL}/I_{OH}$ is measured at $V_{OL}/V_{OH}$ as shown in the dc test configuration.
3. A series termination resistor (Rs) is recommended to help match the source impedance to a 50 W PCB trace. A 5 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3.

**DC Test Configuration**




**AC Test Configuration**

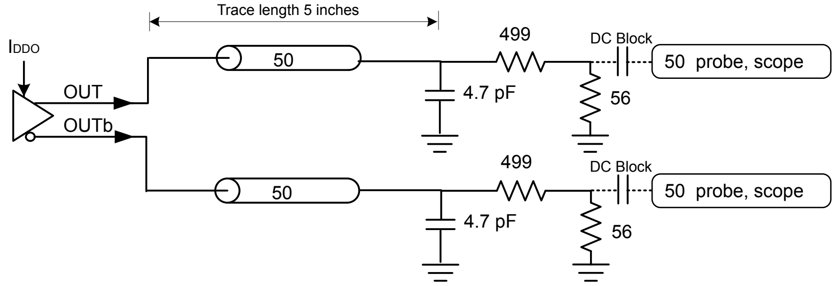


**Table 5.7. Output Status Pin Specifications**

($V_{DD}$=1.8V ± 5%, $V_{DDA}$=3.3V ± 5%, $V_{DDS}$= 3.3V ± 5%, 1.8V ± 5%, $T_A$= -40 to 85°C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Si5341/40 Status Output Pins (INTRb, SDA/SDIO)[1]** | | | | | | |
| Output Voltage | $V_{OH}$ | $I_{OH}$ = -2 mA | $V_{DDIO}$[2] x 0.85 | — | — | V |
| | $V_{OL}$ | $I_{OL}$ = 2 mA | — | — | $V_{DDIO}$[2]x 0.15 | V |
| **Si5341 Status Output Pins (LOLb)** | | | | | | |
| Output Voltage | $V_{OH}$ | $I_{OH}$ = -2 mA | $V_{DDIO}$[2] x 0.85 | — | — | V |
| | $V_{OL}$ | $I_{OL}$ = 2 mA | — | — | $V_{DDIO}$[2] x 0.15 | V |
| **Si5340 Status Output Pins (LOLb, LOS_XAXBb)** | | | | | | |
| Output Voltage | $V_{OH}$ | $I_{OH}$ = -2 mA | $V_{DDS}$ x 0.85 | — | — | V |
| | $V_{OL}$ | $I_{OL}$ = 2 mA | — | — | $V_{DDS}$x 0.15 | V |

**Notes:**
1. The $V_{OH}$ specification does not apply to the open-drain SDA/SDIO output when the serial interface is in I2C mode or is unused with I2C_SEL pulled high. $V_{OL}$ remains valid in all cases.
2. $V_{DDIO}$ is determined by the IO_VDD_SEL bit. It is selectable as $V_{DDA}$ or $V_{DD}$. Refer to the Family Reference Manual for more details on register settings.

**Table 5.8. Performance Characteristics**

($V_{DD}$=1.8V ± 5%, $V_{DDA}$=3.3V ± 5%, $T_A$= -40 to 85°C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CO}$ Frequency Range | $F_{VCO}$ | | 13.5 | — | 14.4 | GHz |
| PLL Loop Bandwidth | $f_{BW}$ | | — | 1.0 | — | MHz |
| Initial Start-Up Time | $t_{START}$ | Time from power-up to when the device generates clocks (Input Frequency >48 MHz) | — | 30 | 45 | ms |
| PLL Lock Time[1] | $t_{ACQ}$ | $f_{IN}$ = 19.44 MHz | 15 | — | 150 | ms |
| Output Delay Adjustment | $t_{DELAY\_frac}$ | $f_{VCO}$ = 14 GHz | — | 0.28 | — | ps |
| | $t_{DELAY\_int}$ | Delay is controlled by the MultiSynth | — | 71.4 | — | ps |
| | $t_{RANGE}$ | | — | ±9.14 | — | ns |
| POR[2] to Serial Interface Ready | $t_{RDY}$ | | — | — | 15 | ms |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Jitter Generation Locked to External Clock[3] | $J_{GEN}$ | Integer Mode[4]<br>12 kHz to 20 MHz | — | 140 | 180 | fs rms |
| | | Fractional/DCO Mode[5]<br>12 kHz to 20 MHz | — | 160 | 210 | fs rms |
| | $J_{PER}$ | Derived from integrated phase noise | — | 110 | — | fs pk-pk |
| | $J_{CC}$ | | — | 180 | — | fs pk |
| | $J_{PER}$ | N = 10,000 cycles Integer or Fractional Mode[4, 5] . Measured in the time domain. Performance is limited by the noise floor of the equipment. | — | 7400 | — | fs pk-pk |
| | $J_{CC}$ | | — | 6700 | — | fs pk |
| Jitter Generation Locked to External XTAL | XTAL Frequency = 48 MHz | | | | | |
| | $J_{GEN}$ | Integer Mode[4]<br>12 kHz to 20 MHz | — | 90 | 140 | fs rms |
| | | Fractional/DCO Mode[5]<br>12 kHz to 20 MHz | — | 115 | 170 | fs rms |
| | $J_{PER}$ | Derived from integrated phase noise | — | 110 | — | fs pk-pk |
| | $J_{CC}$ | | — | 180 | — | fs pk |
| | $J_{PER}$ | N = 10, 000 cycles Integer or Fractional Mode.[4, 5] Measured in the time domain. Performance is limited by the noise floor of the equipment. | — | 7400 | — | fs pk-pk |
| | $J_{CC}$ | | — | 6600 | — | fs pk |
| | XTAL Frequency = 25 MHz | | | | | |
| | $J_{GEN}$ | Integer Mode[4]<br>12 kHz to 20 MHz | | 115 | 140 | fs rms |
| | | Fractional Mode[5]<br>12 kHz to 20 MHz | | 140 | 190 | fs rms |

**Notes:**

1. PLL lock time is measured by first letting the PLL lock, then turning off the input clock, and then turning on the input clock. The time from the first edge of the input clock being re-applied until LOL de-asserts is the PLL lock time.
2. Measured as time from valid $V_{DD}$ and $V_{DD33}$ rails (90% of their value) to when the serial interface is ready to respond to commands. Measured in SPI 4-wire mode, with SCLK @ 10 MHz.
3. Jitter generation test conditions $f_{IN}$ = 100 MHz, $f_{OUT}$ = 156.25 MHz LVPECL.
4. Integer mode assumes that the output dividers (Nn/Nd) are configured with an integer value.
5. Fractional and DCO modes assume that the output dividers (Nn/Nd) are configured with a fractional value and the feedback divider is integer.

**Table 5.9. I²C Timing Specifications (SCL,SDA)**

| Parameter | Symbol | Test Condition | Standard Mode 100 kbps | | Fast Mode 400 kbps | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| SCL Clock Frequency | $f_{SCL}$ | | — | 100 | — | 400 | kHz |
| Hold Time (Repeated) START Condition | $t_{HD:STA}$ | | 4.0 | — | 0.6 | — | µs |
| Low Period of the SCL Clock | $t_{LOW}$ | | 4.7 | — | 1.3 | — | µs |
| HIGH Period of the SCL Clock | $t_{HIGH}$ | | 4.0 | — | 0.6 | — | µs |
| Set-up Time for a Repeated START Condition | $t_{SU:STA}$ | | 4.7 | — | 0.6 | — | µs |
| Data Hold Time | $t_{HD:DAT}$ | | 100 | — | 100 | — | ns |
| Data Set-up Time | $t_{SU:DAT}$ | | 250 | — | 100 | — | ns |
| Rise Time of Both SDA and SCL Signals | $t_r$ | | — | 1000 | 20 | 300 | ns |
| Fall Time of Both SDA and SCL Signals | $t_f$ | | — | 300 | — | 300 | ns |
| Set-up Time for STOP Condition | $t_{SU:STO}$ | | 4.0 | — | 0.6 | — | µs |
| Bus Free Time between a STOP and START Condition | $t_{BUF}$ | | 4.7 | — | 1.3 | — | µs |
| Data Valid Time | $t_{VD:DAT}$ | | — | 3.45 | — | 0.9 | µs |
| Data Valid Acknowledge Time | $t_{VD:ACK}$ | | — | 3.45 | — | 0.9 | µs |

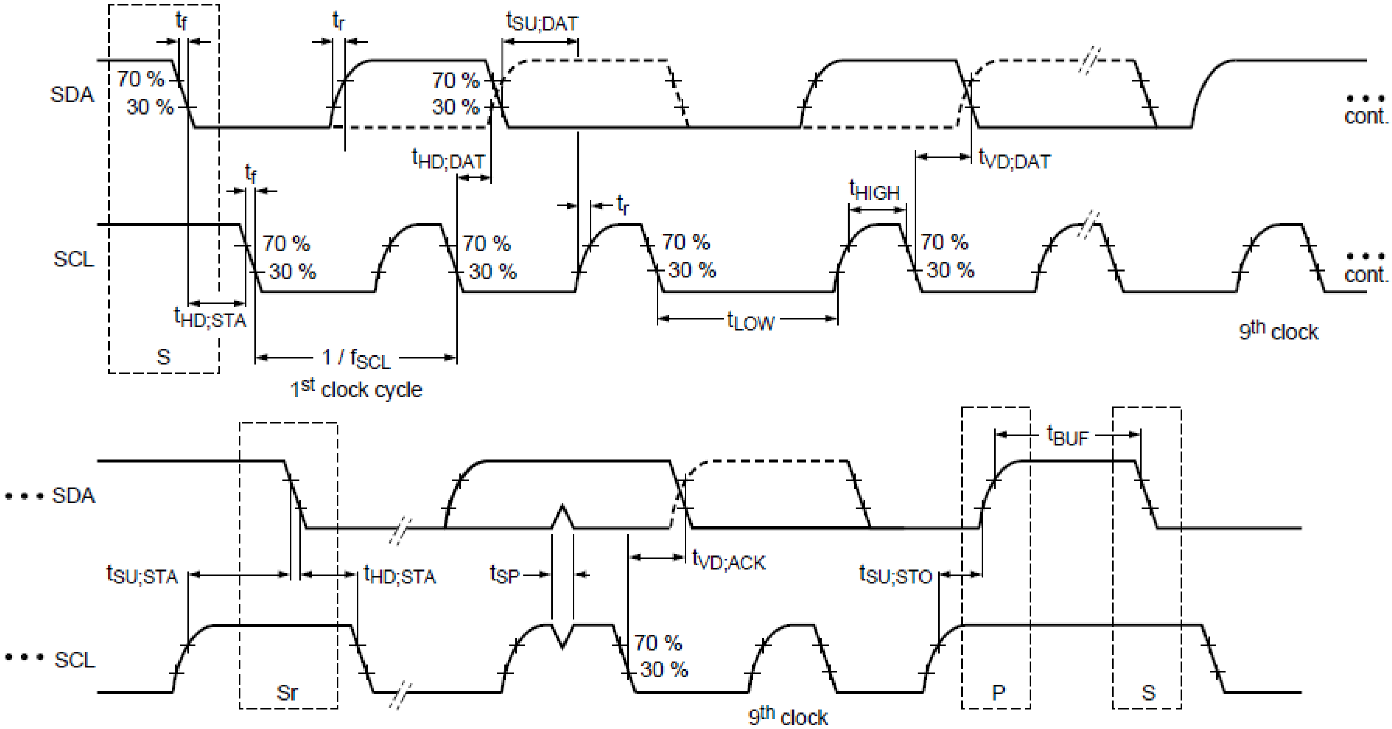



**Figure 5.1. I$^2$C Serial Port Timing Standard and Fast Modes**

**Table 5.10. SPI Timing Specifications (4-Wire)**

($V_{DD}$=1.8V ± 5%, $V_{DDA}$=3.3V ± 5%, $T_A$= -40 to 85°C)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| SCLK Frequency | $f_{SPI}$ | — | — | 20 | MHz |
| SCLK Duty Cycle | $T_{DC}$ | 40 | — | 60 | % |
| SCLK Period | $T_C$ | 50 | — | — | ns |
| Delay Time, SCLK Fall to SDO Active | $T_{D1}$ | — | 12.5 | 18 | ns |
| Delay Time, SCLK Fall to SDO | $T_{D2}$ | — | 10 | 15 | ns |
| Delay Time, CSb Rise to SDO Tri-State | $T_{D3}$ | — | 10 | 15 | ns |
| Setup Time, CSb to SCLK | $T_{SU1}$ | 5 | — | — | ns |
| Hold Time, CSb to SCLK Rise | $T_{H1}$ | 5 | — | — | ns |
| Setup Time, SDI to SCLK Rise | $T_{SU2}$ | 5 | — | — | ns |
| Hold Time, SDI to SCLK Rise | $T_{H2}$ | 5 | — | — | ns |
| Delay Time Between Chip Selects (CSb) | $T_{CS}$ | 2 | — | — | $T_C$ |

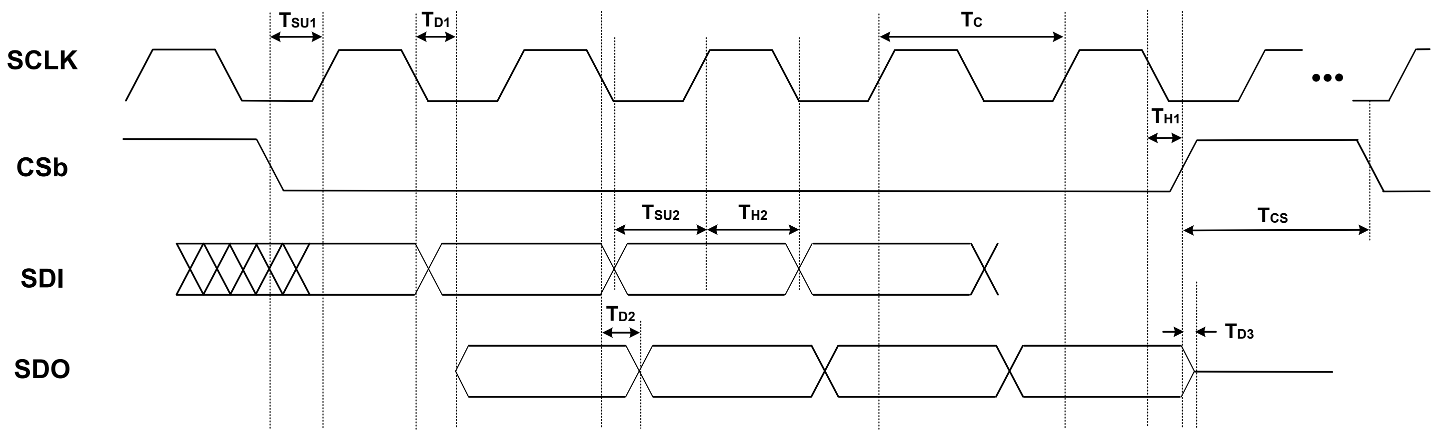



**Figure 5.2. 4-Wire SPI Serial Interface Timing**

**Table 5.11. SPI Timing Specifications (3-Wire)**

($V_{DD}$=1.8V ± 5%, $V_{DDA}$=3.3V ± 5%, $T_A$= -40 to 85°C)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| SCLK Frequency | $f_{SPI}$ | — | — | 20 | MHz |
| SCLK Duty Cycle | $T_{DC}$ | 40 | — | 60 | % |
| SCLK Period | $T_C$ | 50 | — | — | ns |
| Delay Time, SCLK Fall to SDO Turn-on | $T_{D1}$ | — | 12.5 | 20 | ns |
| Delay Time, SCLK Fall to SDO Next-bit | $T_{D2}$ | — | 10 | 15 | ns |
| Delay Time, CSb Rise to SDO Tri-State | $T_{D3}$ | — | 10 | 15 | ns |
| Setup Time, CSb to SCLK | $T_{SU1}$ | 5 | — | — | ns |
| Hold Time, CSb to SCLK Rise | $T_{H1}$ | 5 | — | — | ns |
| Setup Time, SDI to SCLK Rise | $T_{SU2}$ | 5 | — | — | ns |
| Hold Time, SDI to SCLK Rise | $T_{H2}$ | 5 | — | — | ns |
| Delay Time Between Chip Selects (CSb) | $T_{CS}$ | 2 | — | — | $T_C$ |

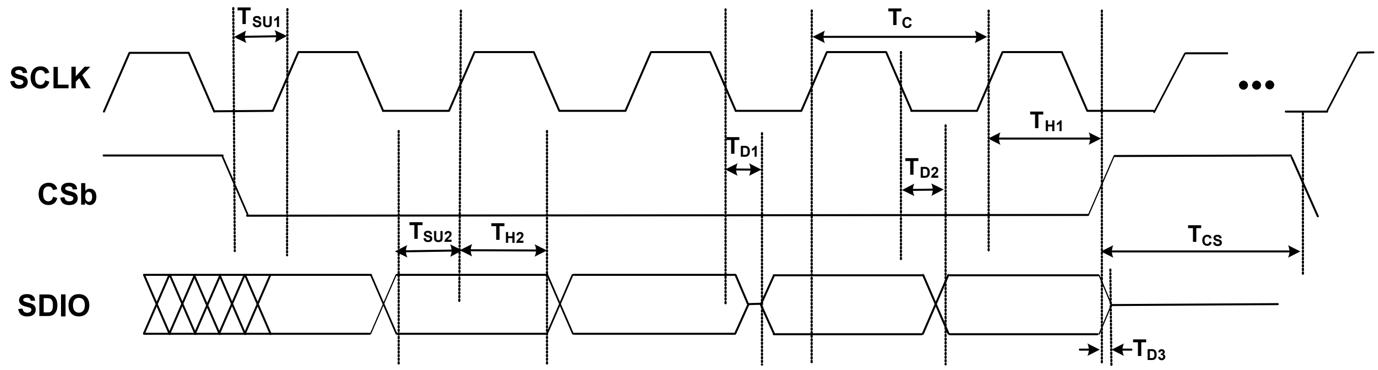



**Figure 5.3. 3-Wire SPI Serial Interface Timing**

**Table 5.12. Crystal Specifications**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Crystal Frequency Range | $f_{XTAL}$ | Full operating range. Jitter performance may be reduced. | 24.97 | — | 54.06 | MHz |
| | | Range for best jitter. | 48 | — | 54 | MHz |
| Load Capacitance | $C_L$ | | — | 8 | — | pF |
| Crystal Drive Level | $d_L$ | | — | — | 200 | μW |
| Equivalent Series Resistance<br>Shunt Capacitance | $r_{ESR}$<br>$C_O$ | Refer to the Si5341/40 Family Reference Manual to determine ESR and shunt capacitance. | | | | |

**Note:**

1. Refer to the Si5341/40 Family Reference Manual for recommended 48 to 54 MHz crystals. The Si5341/40 are designed to work with crystals that meet these specifications.

**Table 5.13. Thermal Characteristics**

| Parameter | Symbol | Test Condition[1] | Value | Units |
|---|---|---|---|---|
| **Si5341 - 64QFN** | | | | |
| Thermal Resistance Junction to Ambient | $\Theta_{JA}$ | Still Air | 22 | °C/W |
| | | Air Flow 1 m/s | 19.4 | |
| | | Air Flow 2 m/s | 18.3 | |
| Thermal Resistance Junction to Case | $\Theta_{JC}$ | | 9.5 | |
| Thermal Resistance Junction to Board | $\Theta_{JB}$ | | 9.4 | |
| | $\Psi_{JB}$ | | 9.3 | |
| Thermal Resistance Junction to Top Center | $\Psi_{JT}$ | | 0.2 | |
| **Si5340 - 44QFN** | | | | |
| Thermal Resistance Junction to Ambient | $\Theta_{JA}$ | Still Air | 22.3 | °C/W |
| | | Air Flow 1 m/s | 19.4 | |
| | | Air Flow 2 m/s | 18.4 | |
| Thermal Resistance Junction to Case | $\Theta_{JC}$ | | 10.9 | |
| Thermal Resistance Junction to Board | $\Theta_{JB}$ | | 9.3 | |
| | $\Psi_{JB}$ | | 9.2 | |
| Thermal Resistance Junction to Top Center | $\Psi_{JT}$ | | 0.23 | |

**Note:**

1. Based on PCB Dimension: 3 x 4.5 mm, PCB Land/Via under GND pad: 36, Number of Cu Layers: 4

**Table 5.14. Absolute Maximum Ratings[1, 2, 3, 4]**

| Parameter | Symbol | Test Condition | Value | Units |
|---|---|---|---|---|
| Storage Temperature Range | $T_{STG}$ | | -55 to +150 | °C |
| DC Supply Voltage | $V_{DD}$ | | -0.5 to 3.8 | V |
| | $V_{DDA}$ | | -0.5 to 3.8 | V |
| | $V_{DDO}$[5] | | -0.5 to 3.8 | V |
| Input Voltage Range | $V_{I1}$ | IN0-IN2, FB_IN | -0.85 to 3.8 | V |
| | $V_{I2}$ | IN_SEL[1:0], RSTb, OEb, SYNCb, I2C_SEL, SDI, SCLK, A0/CSb, A1, SDA/SDIO, FINC/FDEC | -0.5 to 3.8 | V |
| | $V_{I3}$ | XA/XB | -0.5 to 2.7 | V |
| Latch-up Tolerance | LU | | JESD78 Compliant | |
| ESD Tolerance | HBM | 100 pF, 1.5 kΩ | 2.0 | kV |
| Maximum Junction Temperature in Operation | $T_{JCT}$ | | 125 | °C |
| Soldering Temperature (Pb-free profile)[5] | $T_{PEAK}$ | | 260 | °C |
| Soldering Temperature Time at $T_{PEAK}$ (Pb-free profile)[5] | $T_P$ | | 20 to 40 | sec |

**Notes:**

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 64-QFN and 44-QFN packages are RoHS-6 compliant.
3. Moisture sensitivity level is MSL2. For more packaging information, go to the Silicon Labs RoHS information page.
4. The minimum voltage at these pins can be as low as –1.0 V when an AC input signal of 10 MHz or greater is applied. See Table 5.3 Input Clock Specifications on page 20 spec for single-ended AC-coupled $f_{IN}$ < 250 MHz.
5. The device is compliant with JEDEC J-STD-020.

# 6. Typical Application Schematic

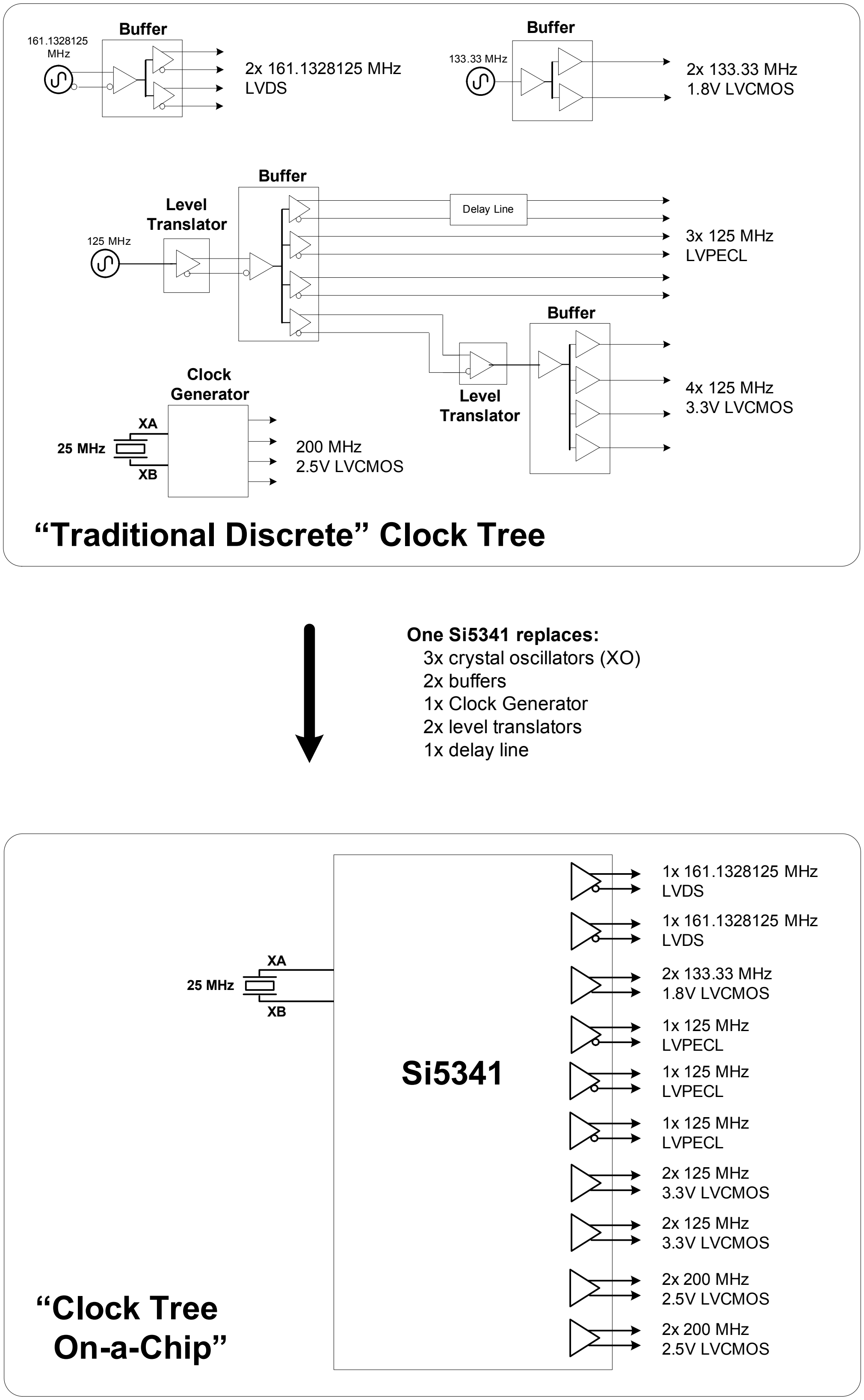



**Figure 6.1. Using the Si5341 to Replace a Traditional Clock Tree**

# 7. Detailed Block Diagrams

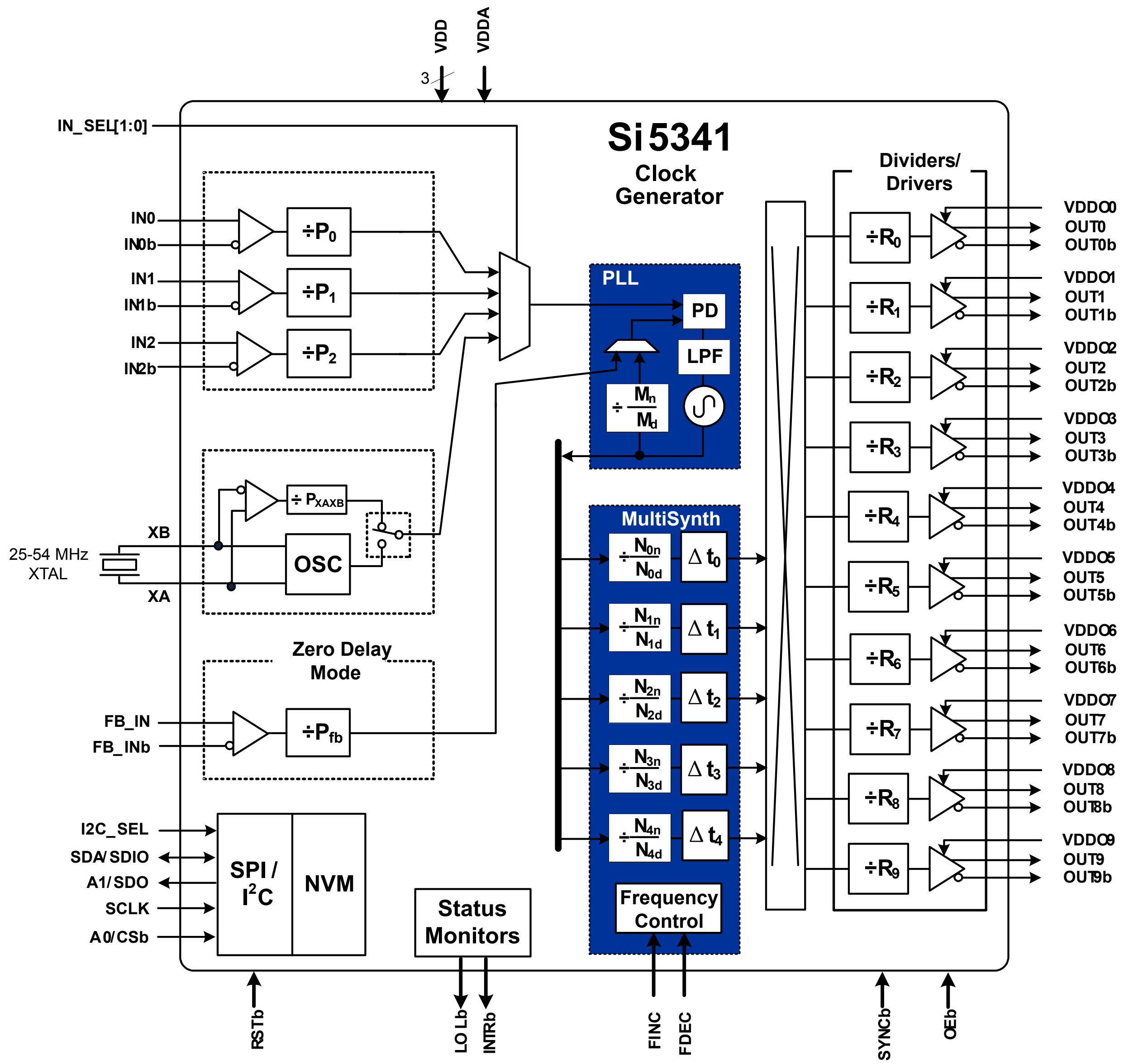



**Figure 7.1. Si5341 Block Diagram**

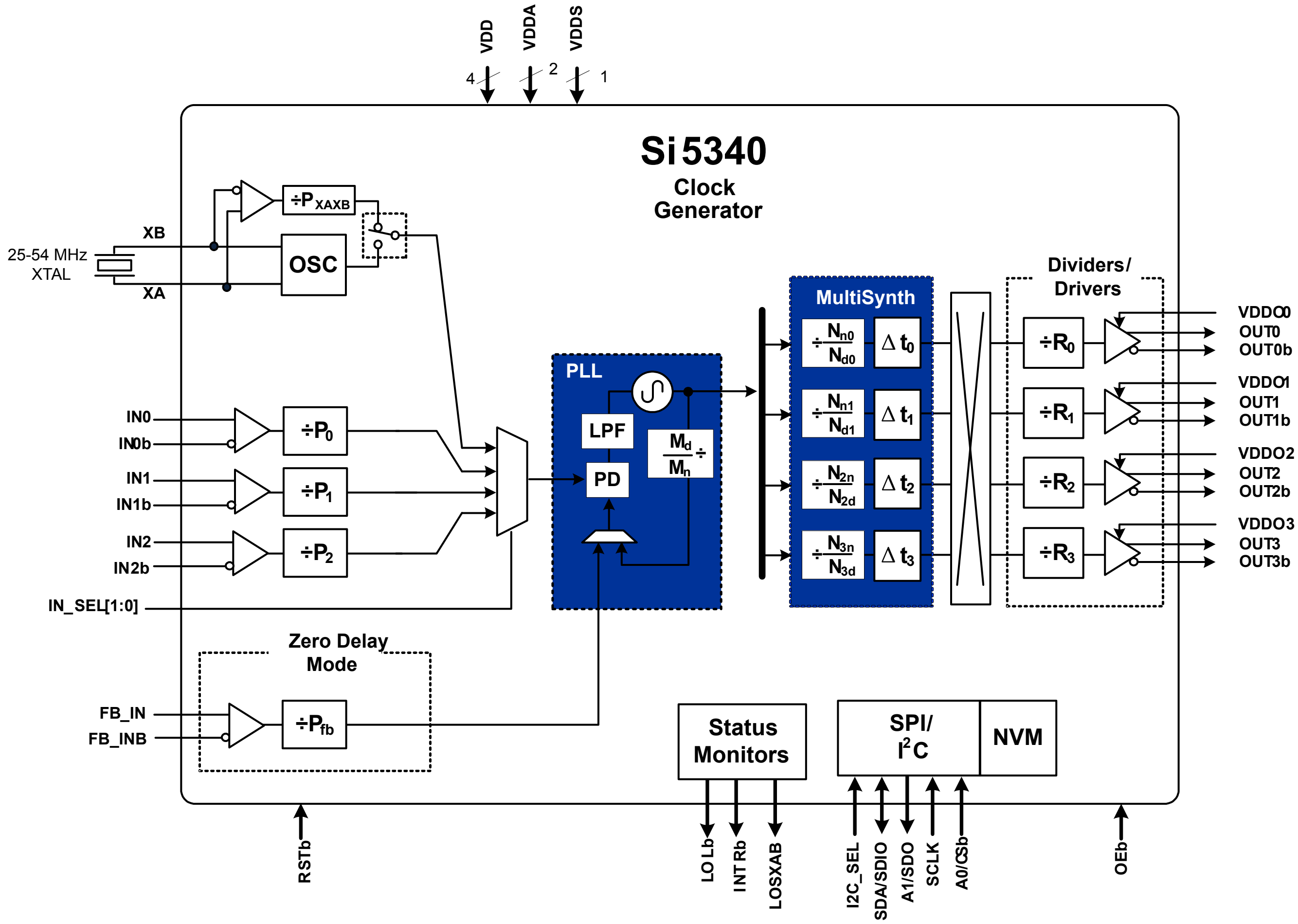



**Figure 7.2. Si5340 Detailed Block Diagram**

## 8. Typical Operating Characteristics

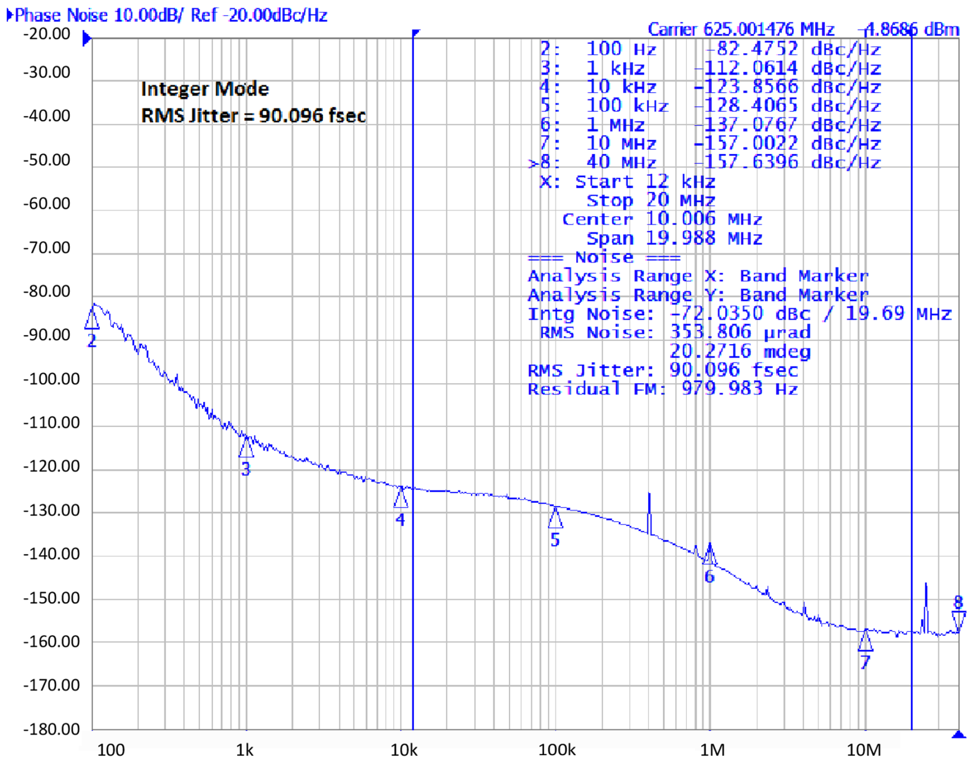



**Figure 8.1. Integer Mode--48 MHz Crystal, 625 MHz Output (2.5 V LVDS)**

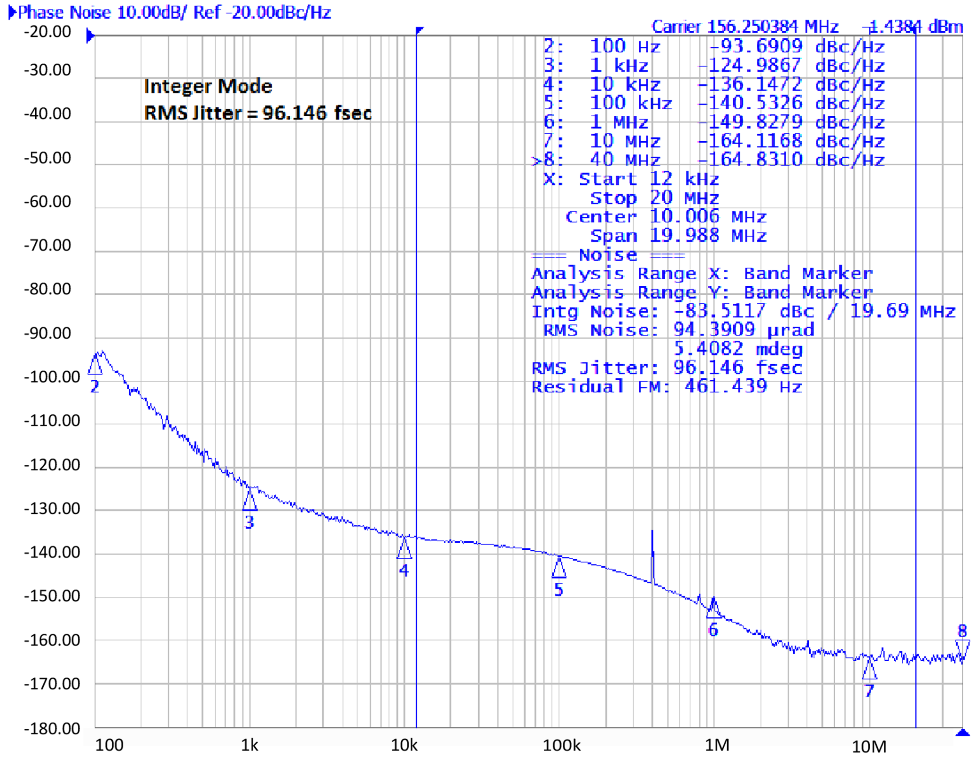



**Figure 8.2. Integer Mode--48 MHz Crystal, 156.25 MHz Output (2.5 V LVDS)**

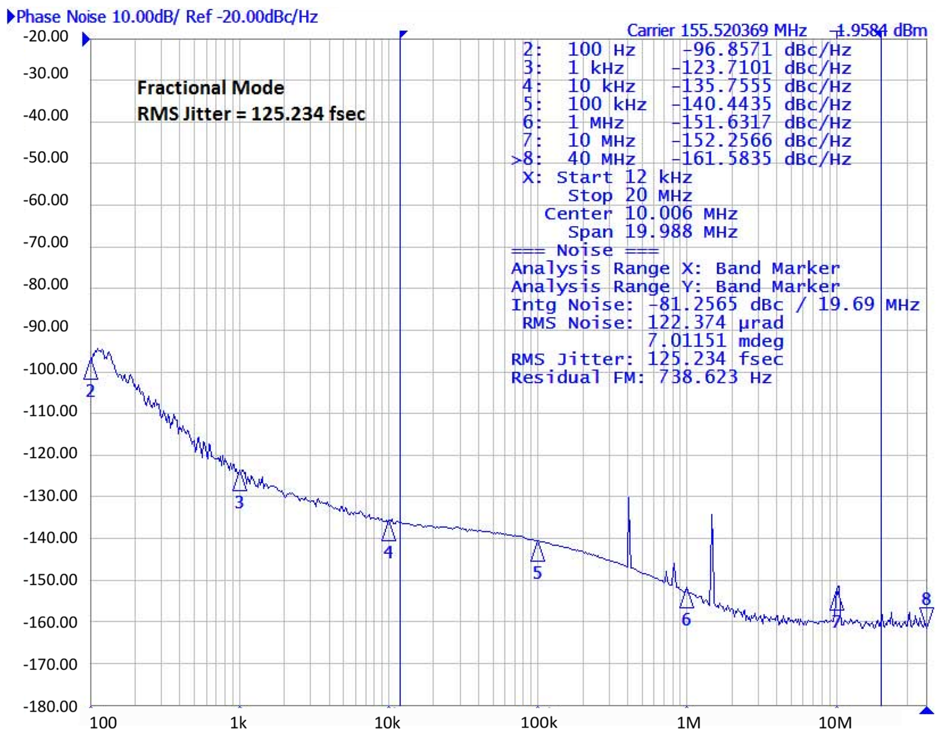
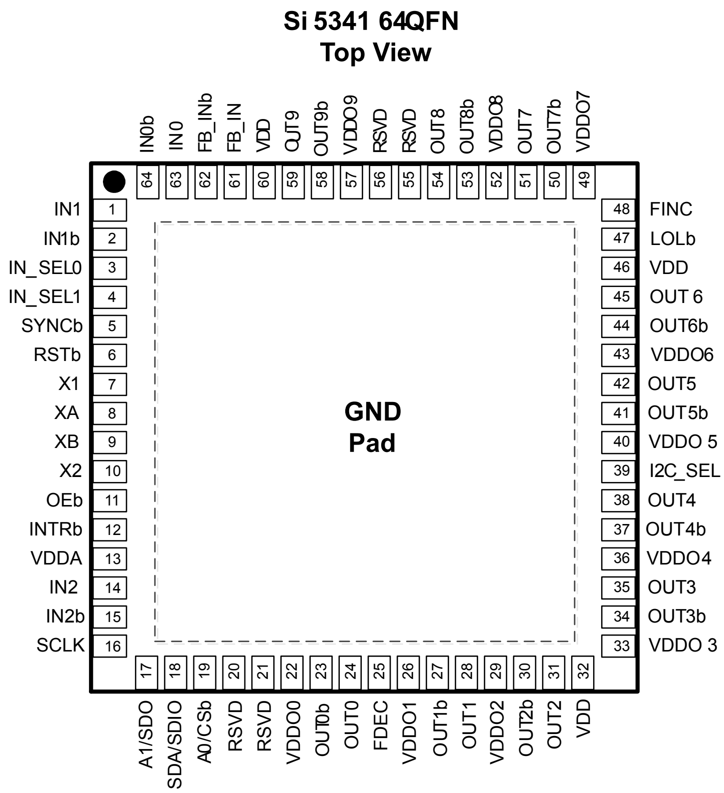



**Figure 8.3. Fractional Mode--48 MHz Crystal, 155.52 MHz Output (2.5 V LVDS)**

## 9. Pin Descriptions



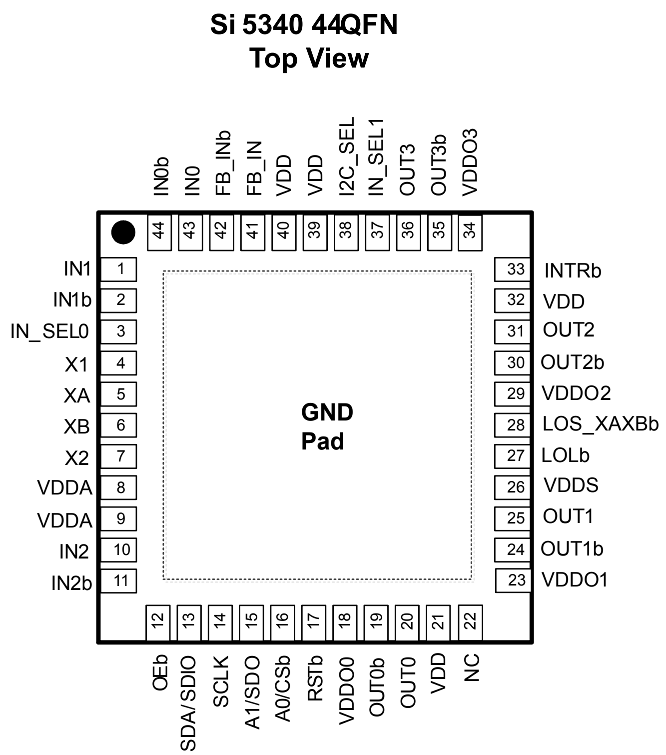



**Table 9.1. Pin Descriptions**

| Pin Name | Pin Number | | Pin Type[1] | Function |
|---|---|---|---|---|
| | Si5341 | Si5340 | | |
| **Inputs** | | | | |
| XA | 8 | 5 | I | **Crystal and External Clock Input.** These pins are used to connect an external crystal or an external clock. See 3.3.1 XA/XB Clock and Crystal Input and Figure 3.2 XAXB External Crystal and Clock Connections on page 5 for connection information. If IN_SEL[1:0] = 11b, then the XAXB input is selected. If the XAXB input is not used and powered down, then both inputs can be left unconnected. ClockBuilder Pro will power down an input that is set as "Unused". |
| XB | 9 | 6 | I | |
| X1 | 7 | 4 | I | **XTAL Shield.** Connect these pins directly to the XTAL ground pins. X1, X2, and the XTAL ground pins must not be connected to the PCB ground plane. DO NOT GROUND THE CRYSTAL GROUND PINS. Refer to the Si5341/40 Family Reference Manual for layout guidelines. These pins should be left disconnected when connecting XA/XB pins to an external reference clock. |
| X2 | 10 | 7 | I | |
| IN0 | 63 | 43 | I | **Clock Inputs.** These pins accept both differential and single-ended clock signals. Refer 3.3.2 Input Clocks (IN0, IN1, IN2) for input termination options. These pins are high-impedance and must be terminated externally. If both the INx and INx (with overstrike) inputs are un-used and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused". |
| IN0b | 64 | 44 | I | |
| IN1 | 1 | 1 | I | |
| IN1b | 2 | 2 | I | |
| IN2 | 14 | 10 | I | |
| IN2b | 15 | 11 | I | |
| FB_IN | 61 | 41 | I | **External Feedback Input.** These pins are used as the external feedback input (FB_IN/FB_INb) for the optional zero delay mode. See 3.5.12 Zero Delay Mode for details on the optional zero delay mode. If FB_IN and FB_IN (with overstrike) are un-used and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused". |
| FB_INb | 62 | 42 | I | |

| Pin Name | Pin Number | | Pin Type[1] | Function |
|---|---|---|---|---|
| | Si5341 | Si5340 | | |
| **Outputs** | | | | |
| OUT0 | 24 | 20 | O | **Output Clocks.** These output clocks support a programmable signal amplitude when configured as a differential output. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.4 LVCMOS Output Terminations. Unused outputs should be left unconnected. |
| OUT0b | 23 | 19 | O | |
| OUT1 | 28 | 25 | O | |
| OUT1b | 27 | 24 | O | |
| OUT2 | 31 | 31 | O | |
| OUT2b | 30 | 30 | O | |
| OUT3 | 35 | 36 | O | |
| OUT3b | 34 | 35 | O | |
| OUT4 | 38 | — | O | |
| OUT4b | 37 | — | O | |
| OUT5 | 42 | — | O | |
| OUT5b | 41 | — | O | |
| OUT6 | 45 | — | O | |
| OUT6b | 44 | — | O | |
| OUT7 | 51 | — | O | |
| OUT7b | 50 | — | O | |
| OUT8 | 54 | — | O | |
| OUT8b | 53 | — | O | |
| OUT9 | 59 | — | O | |
| OUT9b | 58 | — | O | |
| **Serial Interface** | | | | |
| I2C_SEL | 39 | 38 | I | **I$^2$C Select.**[2] This pin selects the serial interface mode as I$^2$C (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled up by a ~ 20 kΩ resistor to the voltage selected by the IO_VDD_SEL register bit. |
| SDA/SDIO | 18 | 13 | I/O | **Serial Data Interface.**[2] This is the bidirectional data pin (SDA) for the I$^2$C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. When in I$^2$C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode. |
| A1/SDO | 17 | 15 | I/O | **Address Select 1/Serial Data Output.**[2] In I$^2$C mode, this pin functions as the A1 address input pin and does not have an internal pull up or pull down resistor. In 4-wire SPI mode this is the serial data output (SDO) pin (SDO) pin and drives high to the voltage selected by the IO_VDD_SEL pin. |
| SCLK | 16 | 14 | I | **Serial Clock Input.**[2] This pin functions as the serial clock input for both I$^2$C and SPI modes.This pin is internally pulled up by a ~20 kΩ resistor to the voltage selected by the IO_VDD_SEL register bit. In I$^2$C mode this pin should have an external pull up of at least 1 kΩ. No pull-up resistor is needed when in SPI mode. |

| Pin Name | Pin Number | | Pin Type[1] | Function |
|---|---|---|---|---|
| | Si5341 | Si5340 | | |
| A0/CSb | 19 | 16 | I | **Address Select 0/Chip Select.**[2] This pin functions as the hardware controlled address A0 in $I^2C$ mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled up by a ~20 kΩ resistor to the voltage selected by the IO_VDD_SEL register bit. |
| **Control/Status** | | | | |
| INTRb | 12 | 33 | O | **Interrupt.** [2] This pin is asserted low when a change in device status has occurred. This interrupt has a push pull output and should be left unconnected when not in use. |
| RSTb | 6 | 17 | I | **Device Reset.** [2] Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled up with a ~20 kΩ resistor to the voltage selected by the IO_VDD_SEL bit. |
| OEb | 11 | 12 | I | **Output Enable.**[2] This pin disables all outputs when held high. This pin is internally pulled low and can be left unconnected when not in use. |
| LOLb | 47 | — | O | **Loss Of Lock.**[2] This output pin indicates when the DSPLL™ is locked (high) or out-of-lock (low). An external pull up or pull down is not needed. |
| | — | 27 | O | **Loss Of Lock.**[3] This output pin indicates when the DSPLL is locked (high) or out-of-lock (low). An external pull up or pull down is not needed. |
| LOS_XAXBb | — | 28 | O | **Loss Of Signal.**[3] This output pin indicates a loss of signal at the XA/XB pins. |
| SYNCb | 5 | — | I | **Output Clock Synchronization.**[2] An active low signal on this pin resets the output dividers for the purpose of re-aligning the output clocks. For a tighter alignment of the clocks, a soft reset should be applied. This pin is internally pulled up with a ~20 kΩ resistor to the voltage selected by the IO_VDD_SEL bit and can be left unconnected when not in use. |
| FDEC | 25 | — | I | **Frequency Decrement Pin.**[2] This pin is used to step-down the output frequency of a selected output. The affected output driver and its frequency change step size is register configurable. This pin is internally pulled low with a ~20 kΩ resistor and can be left unconnected when not in use. |
| FINC | 48 | — | I | **Frequency Increment Pin.**[2] This pin is used to step-up the output frequency of a selected output. The affected output and its frequency change step size is register configurable. This pin is internally pulled low with a ~20 kΩ resistor and can be left unconnected when not in use. |
| IN_SEL0 | 3 | 3 | I | **Input Reference Select.**[2] The IN_SEL[1:0] pins are used in the manual pin controlled mode to select the active clock input. These pins are internally pulled up with a ~20 kΩ resistor to the voltage selected by the IO_VDD_SEL bit and can be left unconnected when not in use. |
| IN_SEL1 | 4 | 37 | I | |
| RSVD | 20 | — | — | **Reserved.** These pins are connected to the die. Leave disconnected. |
| | 21 | — | — | |
| | 55 | — | — | |
| | 56 | — | — | |

| Pin Name | Pin Number | | Pin Type[1] | Function |
|---|---|---|---|---|
| | Si5341 | Si5340 | | |
| NC | — | 22 | — | **No Connect.** These pins are not connected to the die. Leave disconnected. |
| **Power** | | | | |
| VDD | 32 | 21 | P | **Core Supply Voltage.** The device core operates from a 1.8 V supply. A 1.0 µf bypass capacitor is recommended. |
| | 46 | 32 | | |
| | 60 | 39 | | |
| | — | 40 | | |
| VDDA | 13 | 8 | P | **Core Supply Voltage 3.3 V.** This core supply pin requires a 3.3 V power source. A 1.0 µf bypass capacitor is recommended. |
| | — | 9 | P | |
| VDDS | — | 26 | P | **Status Output Voltage.** The voltage on this pin determines the $V_{OL}/V_{OH}$ on LOLb and LOS_XAXBb status output pins. A 0.1 µf to 1.0 µf bypass capacitor is recommended. |
| VDDO0 | 22 | 18 | P | **Output Clock Supply Voltage 0–9.** Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUTx, OUTx outputs. See the Si5341/40 Family Reference Manual for power supply filtering recommendations. Leave VDDO pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. |
| VDDO1 | 26 | 23 | P | |
| VDDO2 | 29 | 29 | P | |
| VDDO3 | 33 | 34 | P | |
| VDDO4 | 36 | — | P | |
| VDDO5 | 40 | — | P | |
| VDDO6 | 43 | — | P | |
| VDDO7 | 49 | — | P | |
| VDDO8 | 52 | — | P | |
| VDDO9 | 57 | — | P | |
| GND PAD | | | P | **Ground Pad** This pad provides electrical and thermal connection to ground and must be connected for proper operation. Use as many vias as practical and keep the via length to an internal ground plan as short as possible. |

**Note:**

1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.
4. Refer to the Family Reference Manual for more information on register setting names.
5. All status pins except I2C and SPI are push-pull.

# 10. Package Outlines

## 10.1 Si5341 9x9 mm 64-QFN Package Diagram

The figure below illustrates the package details for the Si5341. The table below lists the values for the dimensions shown in the illustration.

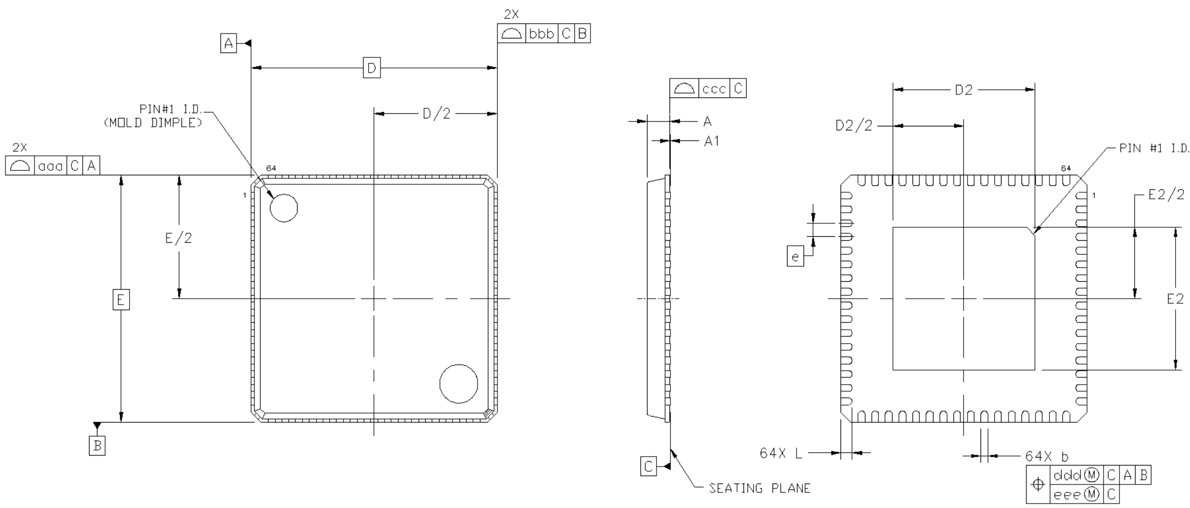



**Figure 10.1. 64-Pin Quad Flat No-Lead (QFN)**

**Table 10.1. Package Dimensions**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| D | 9.00 BSC | | |
| D2 | 5.10 | 5.20 | 5.30 |
| e | 0.50 BSC | | |
| E | 9.00 BSC | | |
| E2 | 5.10 | 5.20 | 5.30 |
| L | 0.30 | 0.40 | 0.50 |
| aaa | — | — | 0.15 |
| bbb | — | — | 0.10 |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.10 |
| eee | — | — | 0.05 |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 10.2 Si5340 7x7 mm 44-QFN Package Diagram

The figure below illustrates the package details for the Si5340. The table below lists the values for the dimensions shown in the illustration.

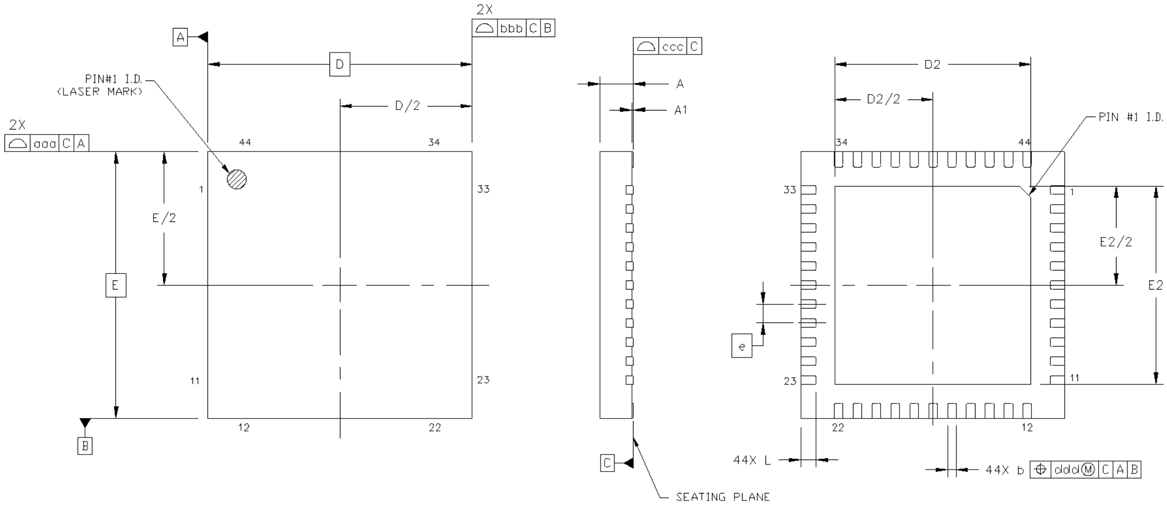



**Figure 10.2. 44-Pin Quad Flat No-Lead (QFN)**

**Table 10.2. Package Dimensions**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| D | | 7.00 BSC | |
| D2 | 5.10 | 5.20 | 5.30 |
| e | | 0.50 BSC | |
| E | | 7.00 BSC | |
| E2 | 5.10 | 5.20 | 5.30 |
| L | 0.30 | 0.40 | 0.50 |
| aaa | — | — | 0.15 |
| bbb | — | — | 0.10 |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.10 |

**Notes:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

# 11. PCB Land Pattern

The figure below illlustrates the PCB land pattern details for the devices. The table below lists the values for the dimensions shown in the illustration.

**Si5341** **Si5340**

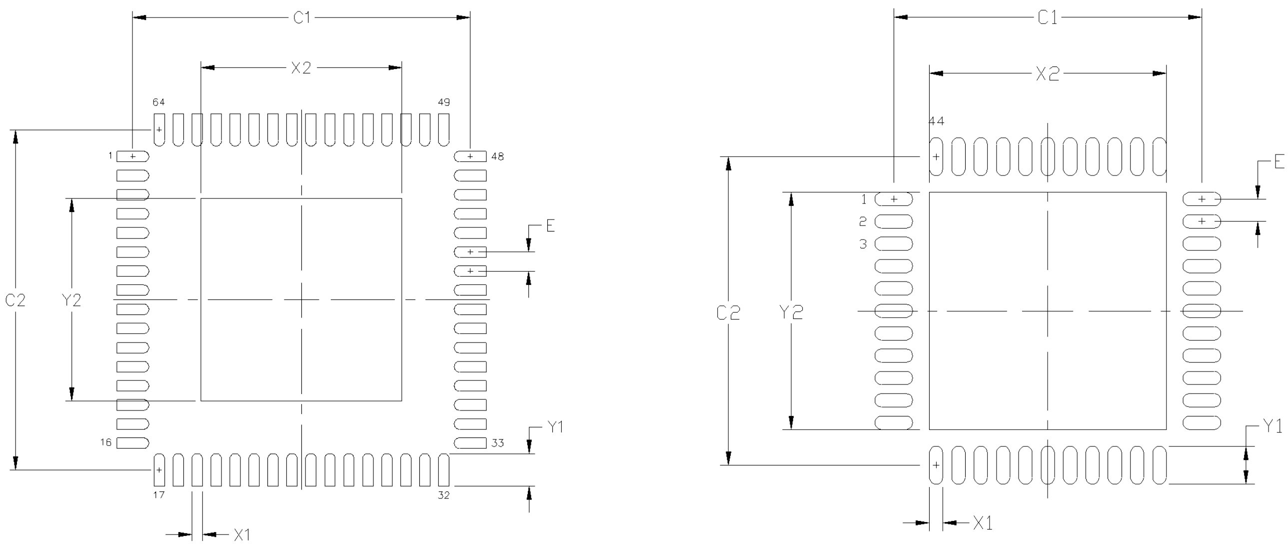



**Figure 11.1. PCB Land Pattern**

**Table 11.1. PCB Land Pattern Dimensions**

| Dimension | Si5341 (Max) | Si5340 (Max) |
|---|---|---|
| C1 | 8.90 | 6.90 |
| C2 | 8.90 | 6.90 |
| E | 0.50 | 0.50 |
| X1 | 0.30 | 0.30 |
| Y1 | 0.85 | 0.85 |
| X2 | 5.30 | 5.30 |
| Y2 | 5.30 | 5.30 |

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication Allowance of 0.05 mm.

**Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

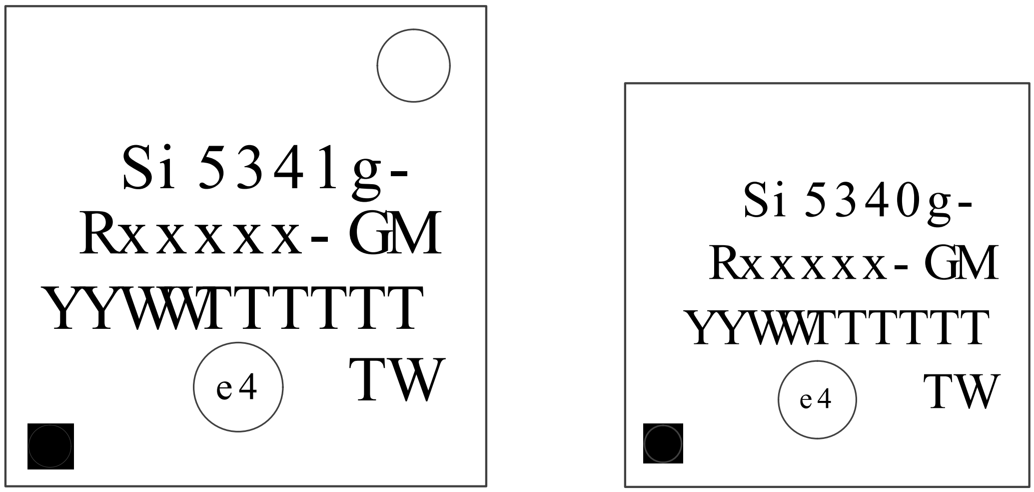
**Stencil Design**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 3×3 array of 1.25 mm square openings on 1.80 mm pitch should be used for the center ground pad.

**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 12. Top Marking




64-QFN 44-QFN

**Figure 12.1. Si5341-40 Top Markings**

**Table 12.1. Si5341-40 Top Marking Explanation**

| Line | Characters | Description |
|---|---|---|
| 1 | Si5341g-<br>Si5340g- | Base part number and Device Grade for Low Jitter, Any-Frequency, 10-output Clock Generator.<br>Si5341: 10-output, 64-QFN<br>Si5340: 4-output, 44-QFN<br>g = Device Grade (A, B, C, D). See " " on page 26 for more information.<br>– = Dash character. |
| 2 | Rxxxxx-GM | R = Product revision. (See ordering guide for current revision).<br>xxxxx = Customer specific NVM sequence number. Optional NVM code assigned for custom, factory pre-programmed devices.<br>Characters are not included for standard, factory default configured devices. See Ordering Guide for more information.<br>–GM = Package (QFN) and temperature range (–40 to +85 °C) |
| 3 | YYWWTTTTTT | YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly.<br>TTTTTT = Manufacturing trace code. |
| 4 | Circle w/ 1.6 mm (64-QFN) or 1.4 mm (44-QFN) diameter | Pin 1 indicator; left-justified |
| | e4<br>TW | Pb-free symbol; Center-Justified<br>TW = Taiwan; Country of Origin (ISO Abbreviation) |

## 13. Device Errata

Please log in or register at www.silabs.com to access the device errata document.

# 14. Document Change List

## 14.1 Revision 1.0

July 15, 2016

- Initial release.

# Table of Contents


## ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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