MIC4478/4479/4480

32V Low-Side Dual MOSFET Drivers

General Description

The MIC4478, MIC4479, and MIC4480 are low-side dual MOSFET drivers are designed to switch N-channel enhancement type MOSFETs from TTL-compatible control signals for low-side switch applications. The MIC4478 is dual non-inverting, the MIC4479 is dual inverting, and the MIC4480 is complimentary non-inverting and inverting. These drivers feature short delays and high peak currents to produce precise edges and rapid rise and fall times.

The MIC4478/4479/4480 are powered from a +4.5V to +32V supply voltage. The on-state gate drive output voltage is approximately equal to the supply voltage (no internal regulators or clamps).

In a low-side configuration, the drivers can control a MOSFET that switches any voltage up to the rating of the MOSFET. The MIC4478/4479/4480 are available in the 8-lead SOIC (ePAD and non-ePAD) package and are rated for the –40°C to +125°C ambient temperature range.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

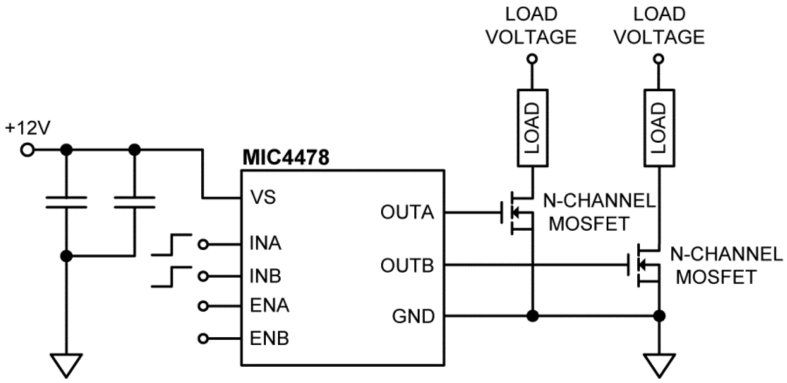
Features

- +4.5V to +32V operation
- 300µA typical supply quiescent current
- 2.5A nominal peak output per channel
  - 6Ω high-side typical output resistance
  - 3Ω low-side typical output resistance
- Active-high driver enable inputs with internal pull-ups
- Operates with low-side switch circuits
- –40°C to +125°C ambient temperature range
- ESD protection
- Dual inverting, dual non-inverting, and inverting + non-inverting versions
- 8-pin SOIC (ePAD and non-ePAD)

Applications

- Synchronous switch-mode power supplies
- Secondary side synchronous rectification

Typical Application



Ordering Information

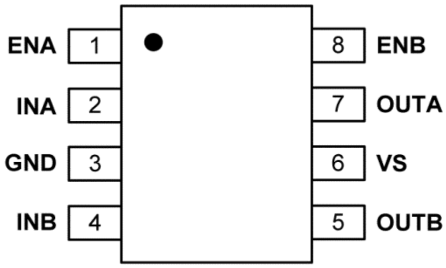
Part Number	Marking	Configuration	Junction Temp. Range	Package	Lead Finish
MIC4478YM	4478YM	Dual Non-Inverting	–40°C to +125°C	8-pin SOIC	Pb-Free
MIC4478YME	4478YME	Dual Non-Inverting	–40°C to +125°C	8-pin ePAD SOIC	Pb-Free
MIC4479YM	4479YM	Dual Inverting	–40°C to +125°C	8-pin SOIC	Pb-Free
MIC4479YME	4479YME	Dual Inverting	–40°C to +125°C	8-pin ePAD SOIC	Pb-Free
MIC4480YM	4480YM	Inverting + Non-Inverting	–40°C to +125°C	8-pin SOIC	Pb-Free
MIC4480YME	4480YME	Inverting + Non-Inverting	–40°C to +125°C	8-pin ePAD SOIC	Pb-Free

Pin Configurations

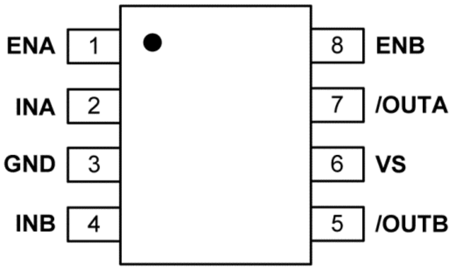
MIC4478: Dual Non-Inverting

MIC4479: Dual Inverting

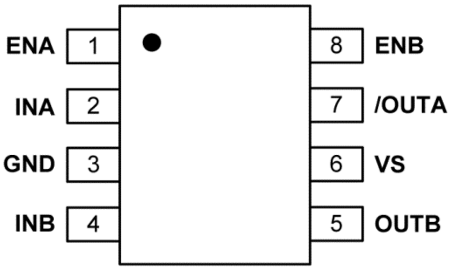
MIC4480: Inverting + Non-Inverting



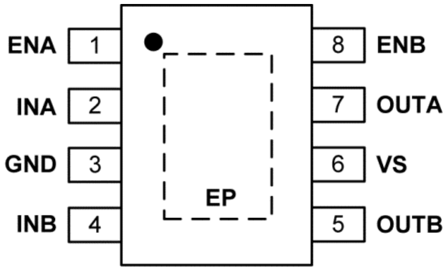
8-Pin SOIC (YM)
(Top View)



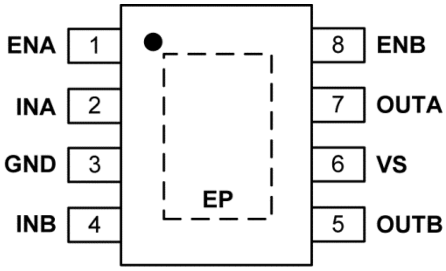
8- Pin SOIC (YM)
(Top View)



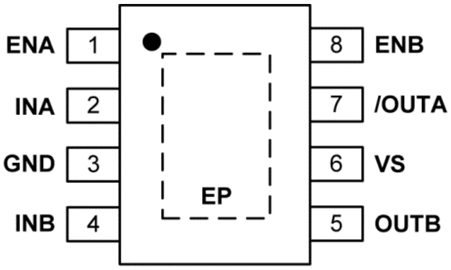
8- Pin SOIC (YM)
(Top View)



8- Pin ePAD SOIC (YME)
(Top View)



8- Pin ePAD SOIC (YME)
(Top View)



8- Pin ePAD SOIC (YME)
(Top View)

Pin Description

Pin Number MIC4478	Pin Number MIC4479	Pin Number MIC4480	Pin Name	Pin Description
1	1	1	ENA	Enable pin channel A. TTL-compatible enabling/disabling of the device. An internal pull-up enables the device if this pin is floating or unconnected. A logic-low voltage disables the device and the output (OUTA) will be pulled to ground regardless of the input state.
2	2	2	INA	Input channel A. TTL-compatible on/off control input. MIC4478 only: A logic-high forces the output (OUTA) to the supply voltage. A logic-low forces OUTA to ground. MIC4479 only: A logic-low forces the output (/OUTA) to the supply voltage. A logic-high forces /OUTA to ground. MIC4480 only: Complimentary logic-low/high (INA/INB) forces the output (/OUTA) to the supply voltage. Complimentary logic-high/high (INA/INB) forces /OUTA to ground.
3	3	3	GND	Ground. Power return.
4	4	4	INB	Input channel B. TTL-compatible on/off control input. MIC4478 only: A logic-high forces the output (OUTB) to the supply voltage. A logic-low forces OUTB to ground. MIC4479 only: A logic-low forces the output (/OUTB) to the supply voltage. A logic-high forces /OUTB to ground. MIC4480 only: Complimentary logic-low/high (INA/INB) forces the output (OUTB) to the supply voltage. Complimentary logic-high/high (INA/INB) forces OUTB to ground.
5	-	5	OUTB	Channel B Output (Non-Inverting). Gate drive connection to the external MOSFET.
-	5	-	/OUTB	Channel B Output (Inverting). Gate drive connection to the external MOSFET.
6	6	6	VS	Supply Input. +4.5V to +32V supply.
7	-	-	OUTA	Channel A Output (Non-Inverting). Gate drive connection to the external MOSFET.
-	7	7	/OUTA	Channel A Output (Inverting). Gate drive connection to the external MOSFET.
8	8	8	ENB	Enable pin channel B. TTL-compatible enabling/disabling of the device. An internal pull-up enables the device if this pin is floating or unconnected. A logic-low voltage disables the device and the output (OUTB) will be pulled to ground regardless of the input state.
EP	EP	EP	ePAD	Ground. Exposed pad of the YME package option. Connect this pad to GND for best thermal performance.

Absolute Maximum Ratings(1)

Supply Voltage (V_S)	–0.3V to +36V
Input Voltage (V_{INA}, V_{INB})	–0.3V to +36V
Enable Voltage (V_{ENA}, V_{ENB})	–0.3V to +36V
Output Voltage (V_{OUTA}, V_{OUTB})	–0.3V to +36V
Junction Temperature (T_J)	150°C
Lead Temperature (soldering, 10s)	260°C
Ambient Storage Temperature (T_S)	–65°C to +150°C
ESD Rating(3)	
Machine Model	200V
Human Body Model	2kV

Operating Ratings(2)

Supply Voltage (V_S)	+4.5V to +32V
Input Voltage (V_{INA}, V_{INB})	0V to V_S
Enable Voltage (V_{ENA}, V_{ENB})	0V to V_S
Ambient Temperature (T_A)	–40°C to +125°C
Junction Thermal Resistance	
8 pin-SOIC (θ_{JA})	63°C/W
8 pin-ePAD SOIC (θ_{JA})	40°C/W

Electrical Characteristics(4)

V_S =12V; T_A = 25°C, **bold** values indicate -40°C ≤ T_J ≤ +125°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Supply						
V_S	Supply Voltage Range		**4.5**		**32**	V
I_S	Quiescent Current	V_{ENA}, V_{ENB} = open; V_{INA}, V_{INB} = 5V/5V (MIC4478)		300	**600**	µA
		V_{ENA}, V_{ENB} = open; V_{INA}, V_{INB} = 0V/0V (MIC4478)				
		V_{ENA}, V_{ENB} = 0V; V_{INA}, V_{INB} = 5V/5V (MIC4478)				
		V_{ENA}, V_{ENB} = 0V; V_{INA}, V_{INB} = 0V/0V (MIC4478)				
		V_{ENA}, V_{ENB} = open; V_{INA}, V_{INB} = 0V/0V (MIC4479)		300	**600**	µA
		V_{ENA}, V_{ENB} = open; V_{INA}, V_{INB} = 5V/5V (MIC4479)				
		V_{ENA}, V_{ENB} = 0V; V_{INA}, V_{INB} = 0V/0V (MIC4479)				
		V_{ENA}, V_{ENB} = 0V; V_{INA}, V_{INB} = 5V/5V (MIC4479)				
		V_{ENA}, V_{ENB} = open; V_{INA}, V_{INB} = 0V/5V (MIC4480)		300	**600**	µA
		V_{ENA}, V_{ENB} = open; $V_{INA,INB}$ = 5V/0V (MIC4480)				
		V_{ENA}, V_{ENB} = 0V; $V_{INA,INB}$ = 0V/5V (MIC4480)				
		V_{ENA}, V_{ENB}=0V; $V_{INA,INB}$ = 5V/0V (MIC4480)				
Input						
$V_{INA,INB}$	Input Voltage	V_{INA}, V_{INB} → logic 1 input	**2.4**			V
		V_{INA}, V_{INB} → logic 0 input			**0.8**	V
		Hysteresis voltage		0.3		V
$I_{INA,INB}$	Input Current	0V ≤ $V_{INA,INB}$ ≤ V_S	**–10**		**10**	µA
$t_{RD,INA,INB}$	Rising delay time: $V_{INA,INB}$ to V_{OUTA}, V_{OUTB}	V_S = 12V; C_L = 1000Pf			160	ns
		V_S = 30V; C_L = 1000pF			160	ns
$t_{FD,INA,INB}$	Falling delay time: V_{INA}, V_{INB} to V_{OUTA}, V_{OUTB}	V_S = 12V; C_L = 1000pF			70	ns
		V_S = 30V; C_L = 1000pF			70	ns

Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5kΩ in series with 100pF.
4. Specification for packaged product only.

Electrical Characteristics(4) (Continued)

V_S = 12V; T_J = 25°C, **bold** values indicate -40°C ≤ T_J ≤ +125°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Enable						
V_{ENA}, V_{ENB}	Enable Voltage	V_{EN} logic 1 input	**2.4**			V
		V_{EN} logic 0 input			**0.8**	V
		Hysteresis voltage		0.3		V
I_{ENA}, I_{ENB}	Enable Current	0V ≤ V_{ENA}, V_{ENB} ≤ V_S	**-10**		**10**	µA
Output						
t_R	Rise Time: Output V_{OUTA}, V_{OUTB}	V_S = 12V; C_L = 1000pF			120	ns
		V_S = 30V; C_L = 1000pF			120	ns
t_F	Fall Time: Output V_{OUTA}, V_{OUTB}	V_S = 12V; C_L = 1000pF			45	ns
		V_S = 30V; C_L = 1000pF			45	ns
Z_{OUTA}, Z_{OUTB}	Output Resistance	PMOS: V_S = 12V, I_{OUT} = 100mA		6		Ω
		NMOS: V_S = 12V, I_{OUT} = 100mA		3		Ω
$I_{OUT\ REVERSE}$	Output Reverse Current	No latch up		250		mA

Timing Diagram

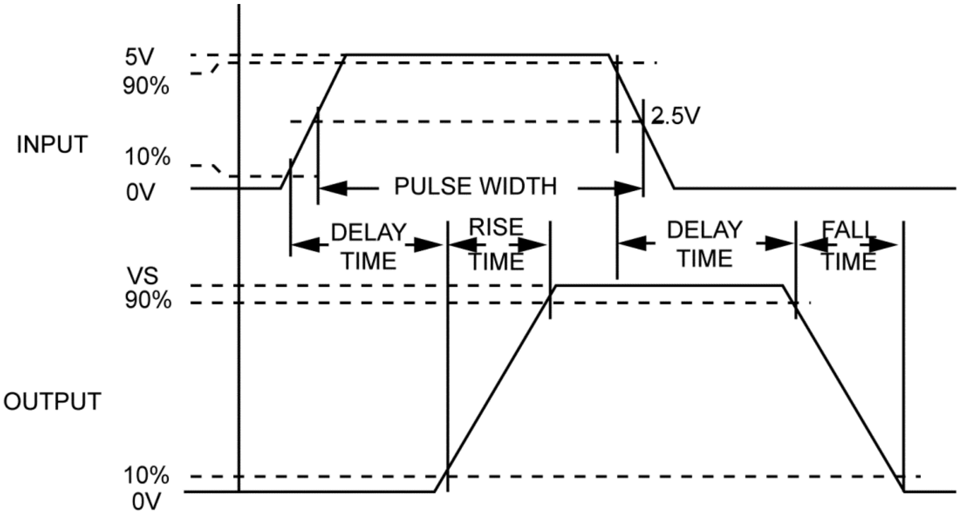


Figure 1. MIC4478/4480 (Non-Inverting) Timing Diagram

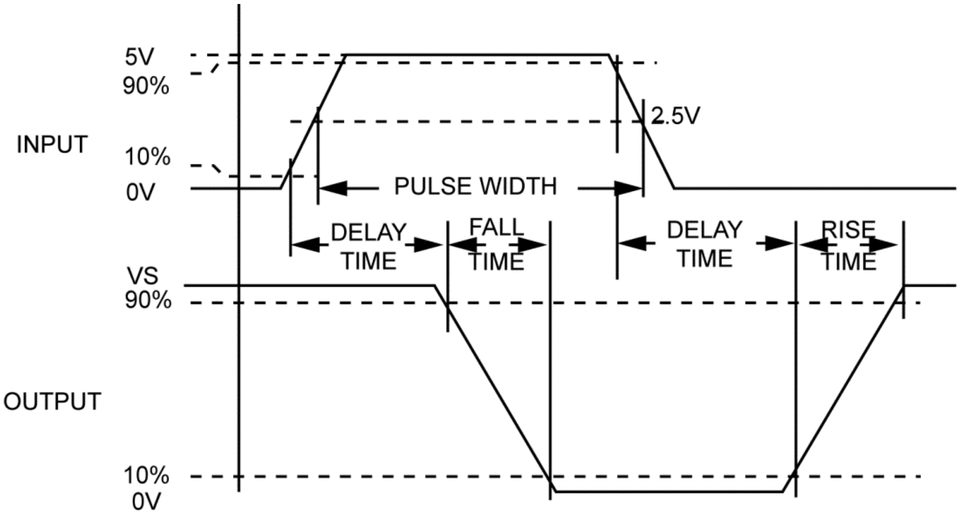


Figure 2. MIC4479/4480 (Inverting) Timing Diagram

Functional Diagram

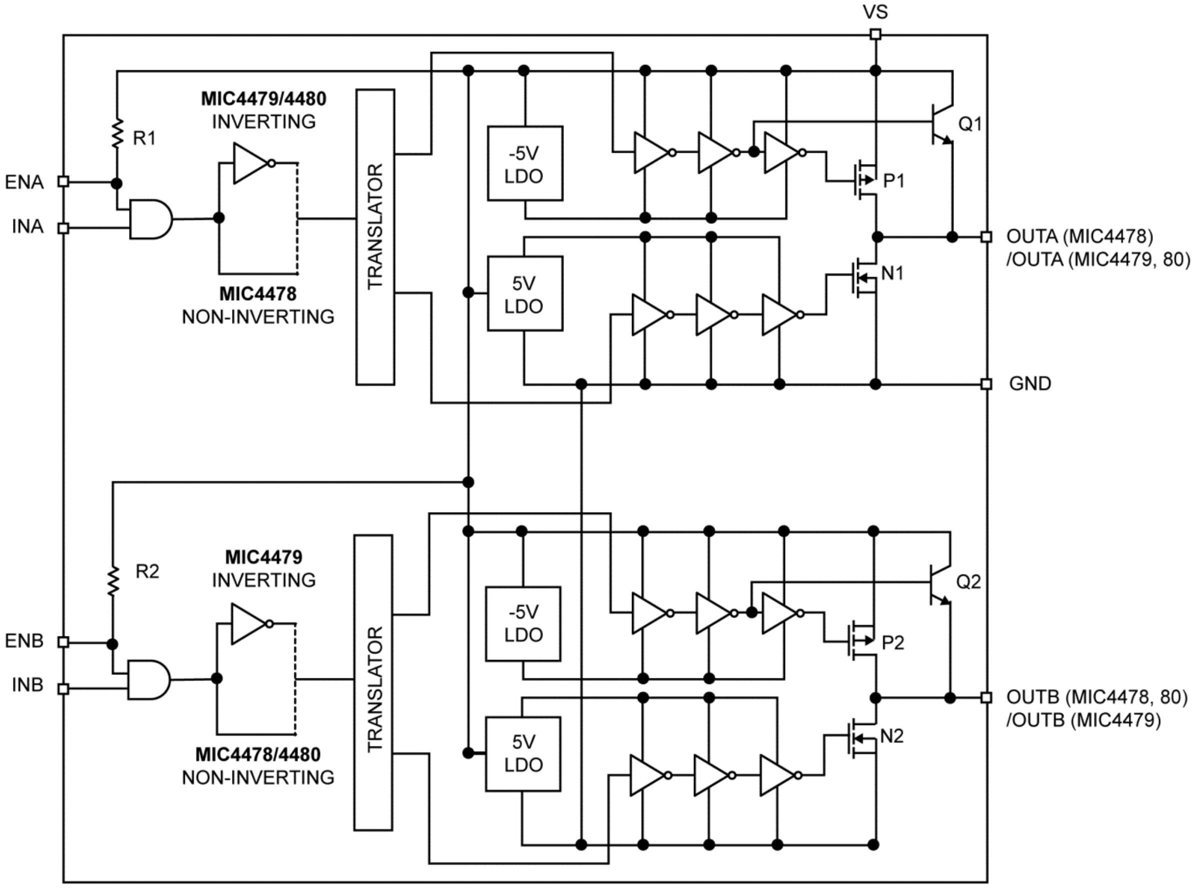
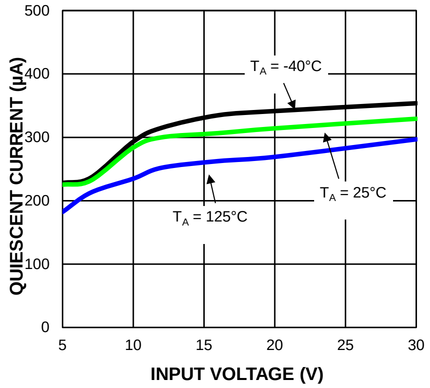
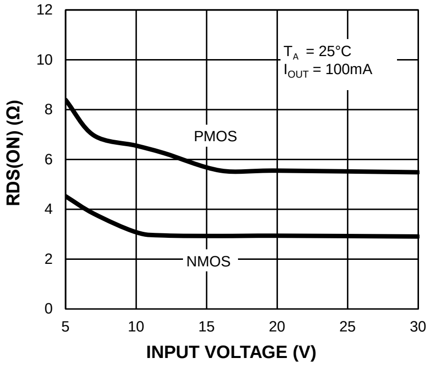
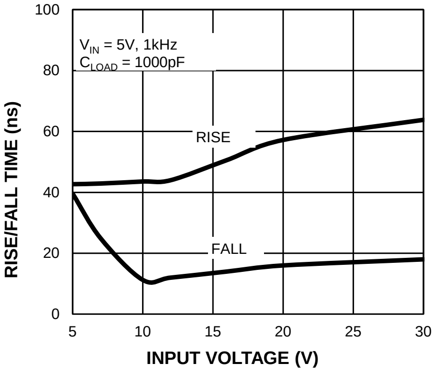


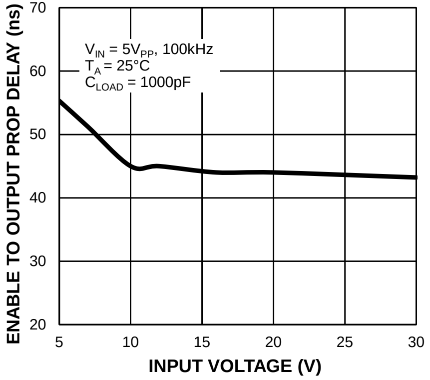
Figure 3. Simplified MIC4478/4479/4480 Functional Block Diagram

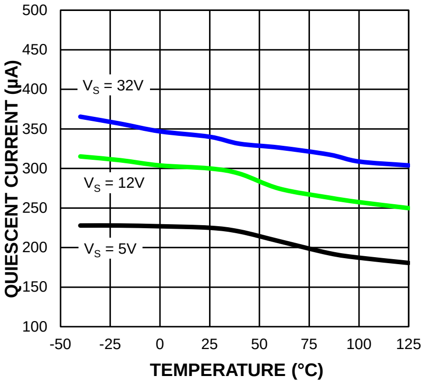
Typical Characteristics

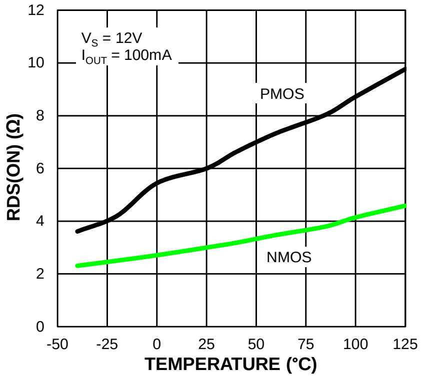

Quiescent Current vs. Input Voltage

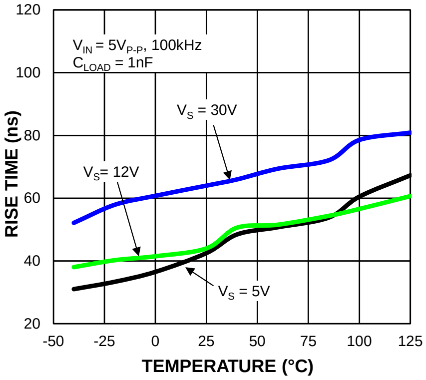

Output Resistance vs. Input Voltage

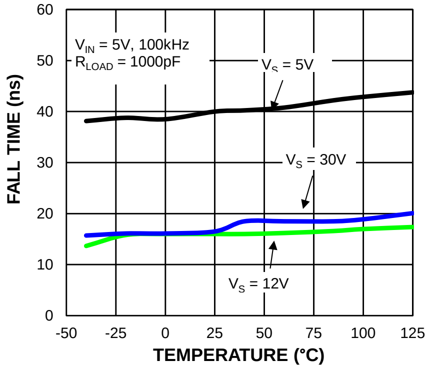

Rise/Fall Time vs. Input Voltage

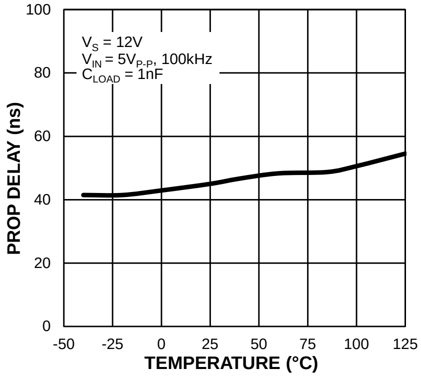

Enable to Output Propagation Delay vs. Input Voltage


Quiescent Current vs. Temperature

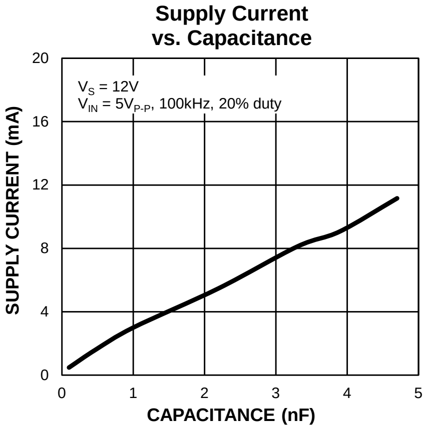

Output Resistance vs. Temperature

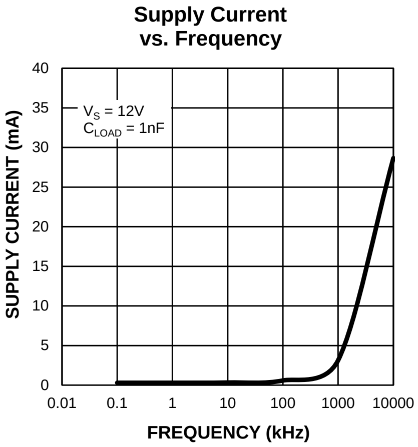

Rise Time vs. Temperature


Fall Time vs. Temperature


Enable-to-Output Propagation Delay vs. Temperature

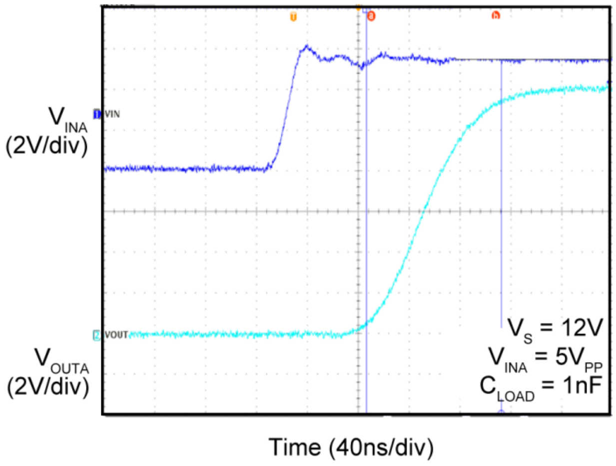
Typical Characteristics (Continued)



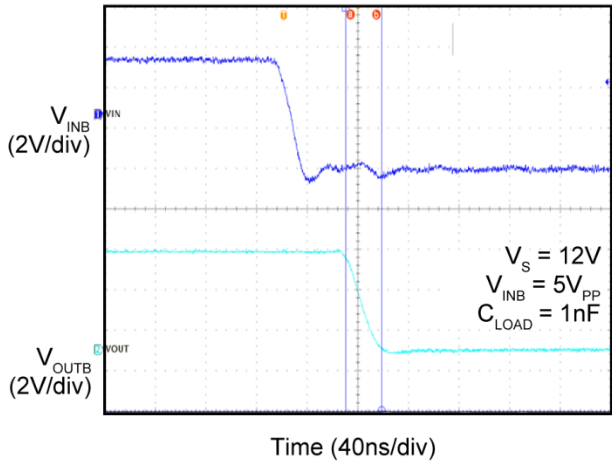


Functional Characteristics

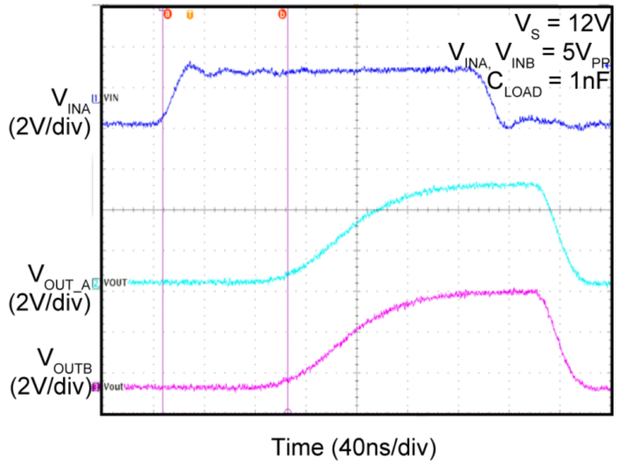
V_{OUTA} Rise Time - V_S = 12V



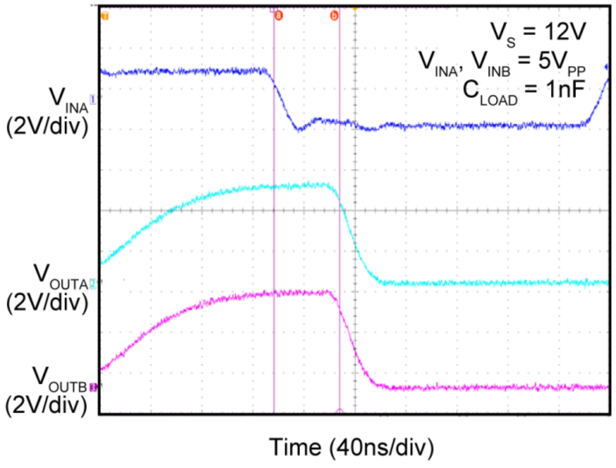
V_{OUTB} Fall Time - V_S = 12V



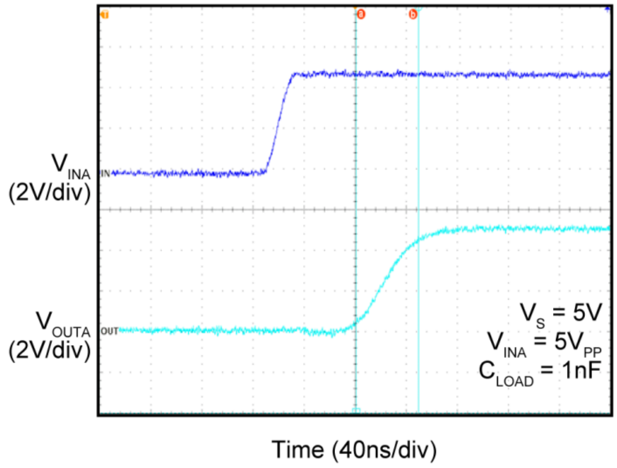
V_{OUTA}, V_{OUTB} Rise and Delay Times



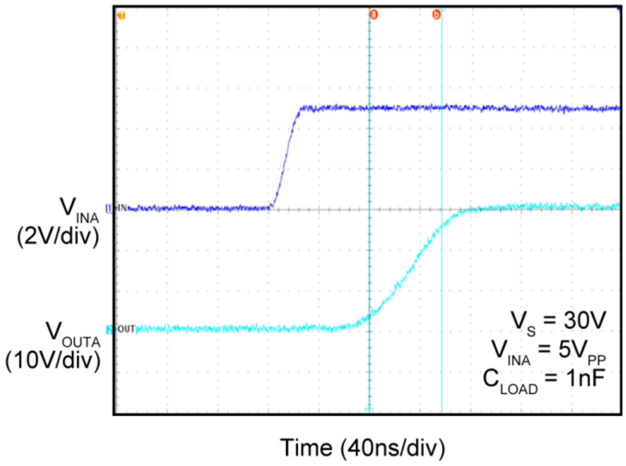
V_{OUTA}, V_{OUTB} Fall and Delay Times



V_{OUTA} Rise Time - V_S = 5V

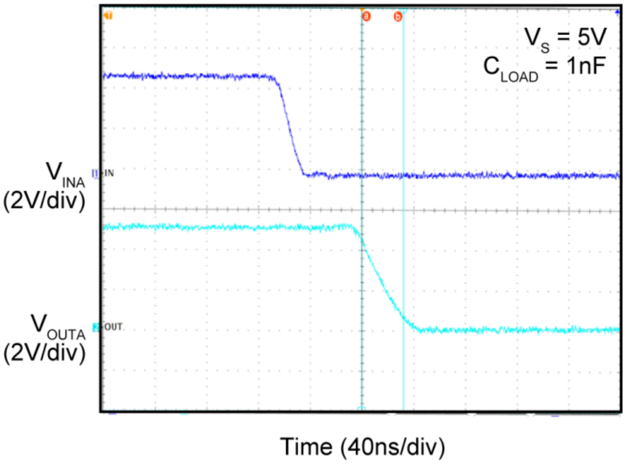


V_{OUTA} Rise Time - V_S = 30V

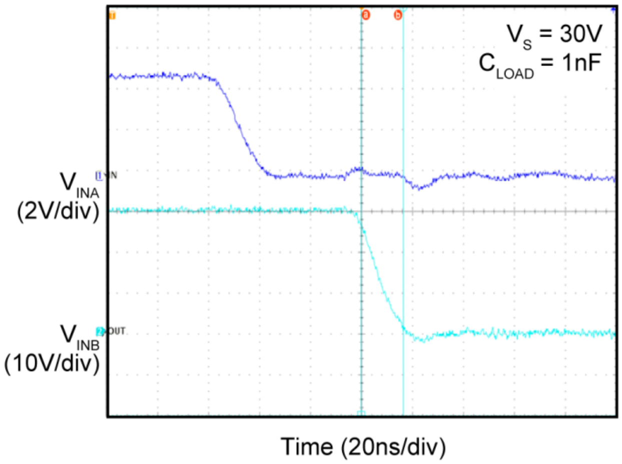


Functional Characteristics (Continued)

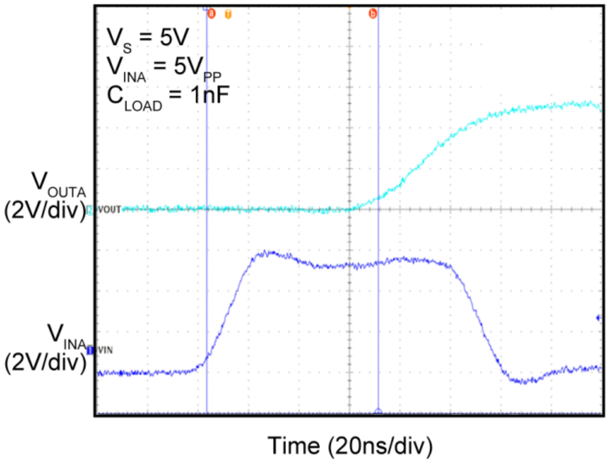
V_{OUTA} Fall Time - V_S = 5V



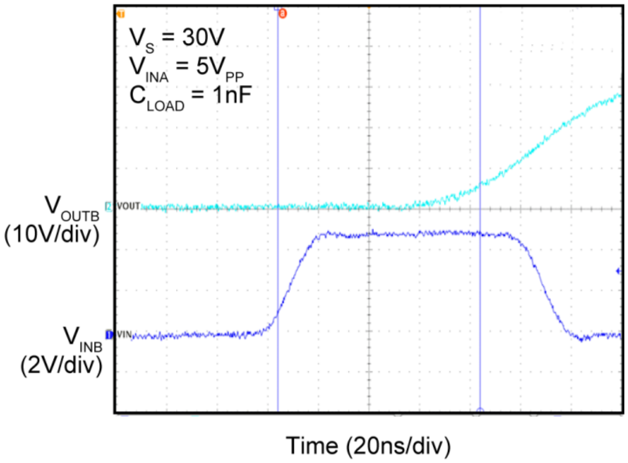
V_{OUTA} Fall Time - V_S = 30V



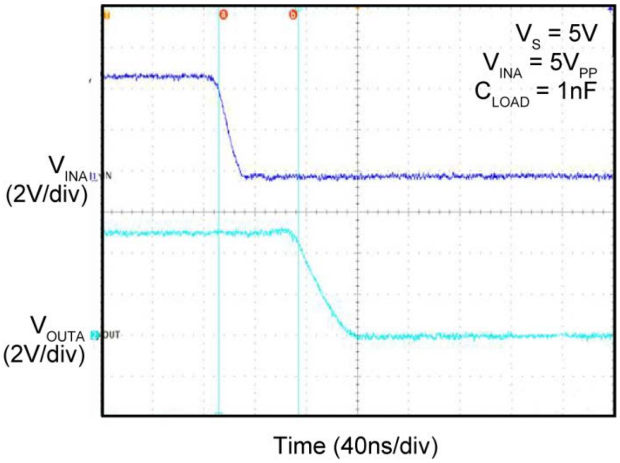
V_{OUTA} Delay Time - V_S = 5V



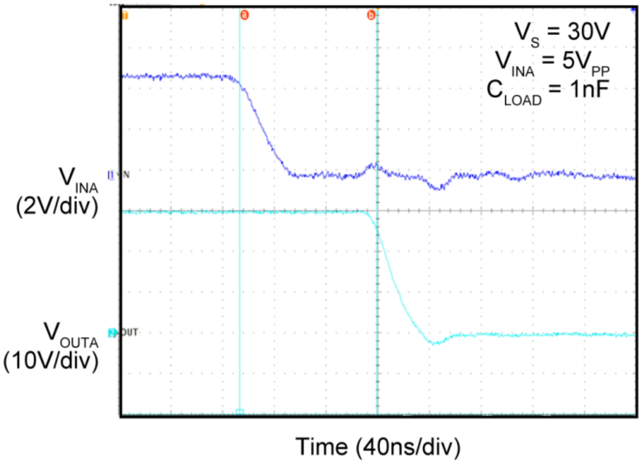
V_{OUTB} Delay Time - V_S = 30V



V_{OUTA} (Falling - OFF) Delay Time - V_S = 5V

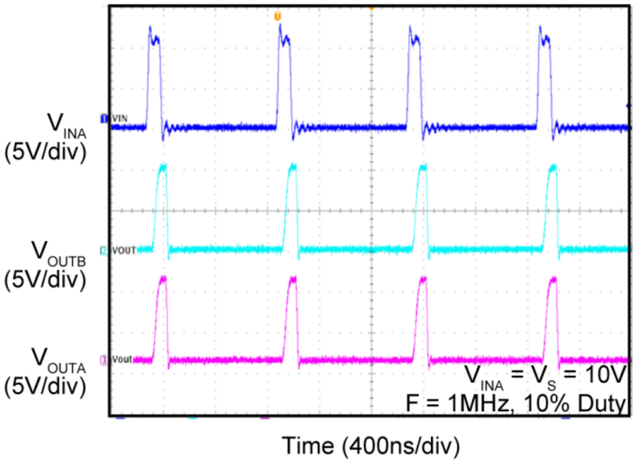


V_{OUTA} (Falling - OFF) Delay Time - V_S = 30V

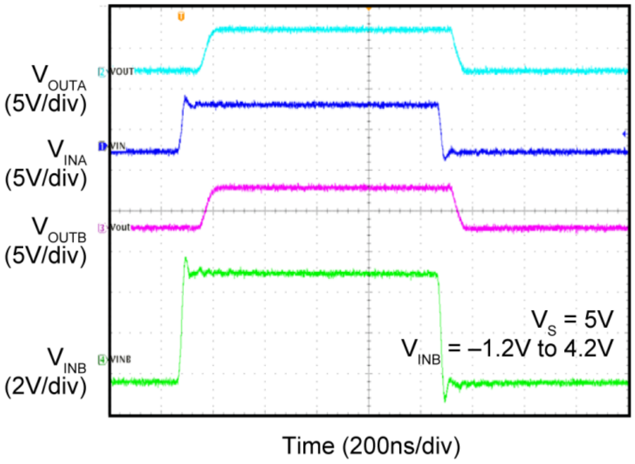


Functional Characteristics (Continued)

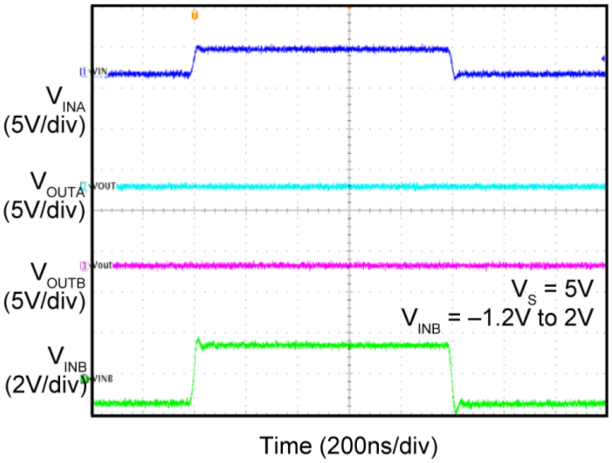
Steady State Operation



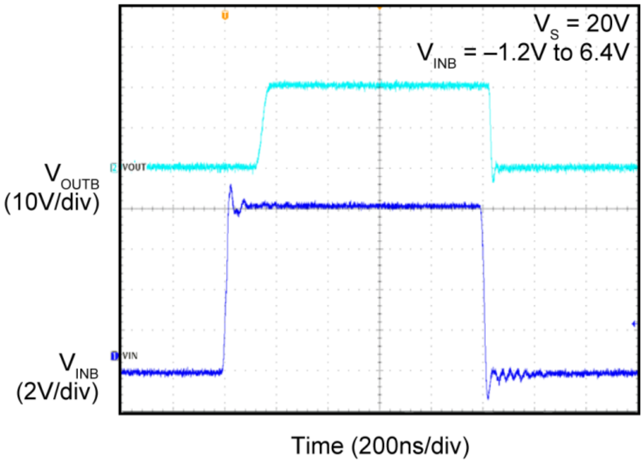
V_{IN} Positive and Negative Output



V_{IN} Negative Input Swing - No Output



V_{IN} Positive and Negative Input - V_S = 20V



Functional Description

The MIC4478 is a dual non-inverting driver. A logic-high on the INA, INB (input) pins produce gate drive outputs. The MIC4479 is a dual-inverting driver. A logic-low on the INA, INB (input) pins produce gate drive outputs. The MIC4480 is a complimentary inverting and non-inverting driver, a logic-low and high on the INA, INB (input) pins produce gate drive outputs. The OUTA, OUTB (output) pins are used to turn on external N-channel MOSFETs.

Supply

Voltage supply (VS) is rated for +4.5V to +32V. External ceramic capacitors are recommended to decouple noise. See Supply Bypass in the Application Information section.

Input

INA, INB (inputs) are TTL-compatible inputs. INA, INB must be forced high or low by an external signal. A floating input will cause unpredictable operation.

Enable

Each output has an independent enable pin that forces the output low when the enable pin is driven low. Each enable pin is internally pulled-up to VS. The outputs are enabled by default if the enable pin is left open. Pulling the enable pin low, below its threshold voltage, forces the output low. A fast propagation delay between the enable and output pins quickly disables the output, which is a requirement during a system fault condition.

Output

The OUTA, OUTB outputs are designed to drive capacitive loads. $V_{OUTA,\ OUTB}$ output voltages will either be the supply voltage or ground voltage, depending on the logic state applied to INA/INB.

If INA, INB are logic-high, and VS drops to zero, the output will be floating and unpredictable.

Application Information

The MIC4478/4479/4480 driver family is designed to provide high peak current for charging and discharging capacitive loads.

Supply Bypass

Capacitors from VS to GND are recommended to control switching and supply transients. Load current and supply lead length are some of the factors that affect capacitor size requirements.

A 4.7µF or 10µF ceramic capacitor is suitable for many applications. Low equivalent series resistance (ESR) metalized film capacitors may also be suitable. An additional 0.1µF ceramic capacitor is suggested in parallel with the larger capacitor to control high-frequency transients.

Circuit Layout

Avoid long power supply and ground traces. They exhibit inductance that can cause voltage transients (inductive kick). Even with resistive loads, inductive transients can sometimes exceed the ratings of the MOSFET and the driver.

When a load is switched off, supply lead inductance forces the current to continue flowing, resulting in a positive voltage spike. Inductance in the ground (return) lead to the supply has similar effects, except that the voltage spike is negative. Switching transitions momentarily draw current from VS to GND. This combines with supply lead inductance to create voltage transients at turn-on and turn-off.

Transients can also result in slower apparent rise or fall times when driver's ground shifts with respect to the control input. Minimize the length of supply and ground traces or use ground and power planes when possible. Bypass capacitors should be placed as close as practical to the driver.

MOSFET Selection

Standard MOSFETs

A standard N-channel power MOSFET is fully enhanced with a gate-to-source voltage of approximately 10V and has an absolute maximum gate-to-source voltage of ±20V. The MIC4478/4479/4480's on-state outputs are approximately equal to the supply voltage. The lowest usable voltage depends upon the behavior of the MOSFETs.

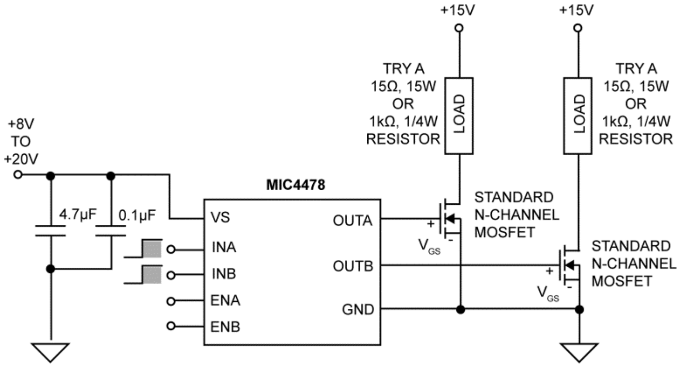


Figure 4. Using Standard N-Channel MOSFETs

Logic-Level MOSFETs

Logic-level N-channel power MOSFETs are fully enhanced with a gate-to-source voltage of approximately 5V and have an absolute maximum gate-to-source voltage of ±10V. They are less common and generally more expensive. The MIC4478/4479/4480 can drive logic-level MOSFETs if the supply voltage, including transients, does not exceed the maximum MOSFET gate-to-source rating (10V).

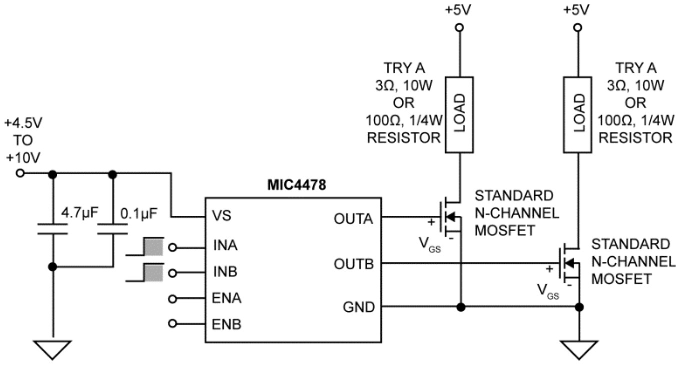


Figure 5. Using Logic-Level N-Channel MOSFETs

At low voltages, the MIC4478/4479/4480's internal P- and N-channel MOSFET's on-resistance will increase and slow the output rise time. Refer to the Typical Characteristics graphs.

Inductive Loads

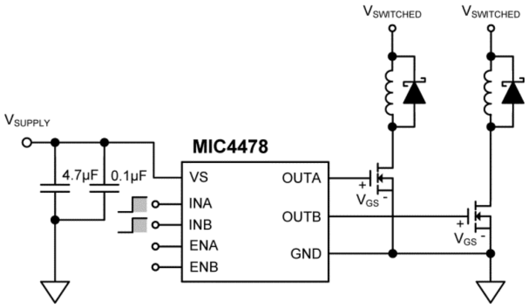


Figure 6. Switching an Inductive Load

Switching off an inductive load in a low-side application forces the MOSFET drain higher than the supply voltage (as the inductor resists changes to current). To prevent exceeding the MOSFET's drain-to-gate and drain-to-source ratings, a Schottky diode should be connected across the inductive load.

Power Dissipation

The maximum power dissipation must not be exceeded to prevent die meltdown or deterioration.

Power dissipation in on/off switch applications is negligible.

Fast repetitive switching applications, such as switch-mode power supplies (SMPS), cause a significant increase in power dissipation with frequency. Power is dissipated each time current passes through the internal output MOSFETs when charging or discharging the external MOSFET. Power is also dissipated during each transition when some current momentarily passes from VS to GND through both internal MOSFETs.

Total power dissipation is the product of supply voltage and supply current plus the product of the gate capacitance of the external MOSFET, supply voltage squared, and the switching frequency:

1) Static Power Dissipation → $P_{D(static)} = V_S \times I_S$

where:

$P_{D(static)}$ = static power dissipation (W)

V_S = supply voltage (V)

I_S = supply current (A)

Supply current is a function of supply voltage, switching frequency, and load capacitance. Determine this value from the "Typical Characteristics: Supply Current vs. Frequency" graph or measure it in the actual application.

T_J (junction temperature) is the sum of T_A (ambient temperature) and the temperature rise across the thermal resistance of the package. In another form:

2) Dynamic Power Dissipation → $P_{D(dynamic)} = V_S^2 \times C_G \times f$

where:

$P_{D(dynamic)}$ = dynamic power dissipation (W)

V_S = supply voltage (V)

C_G = gate capacitance of external MOSFET (µF)

f = switching frequency (Hz)

Do not allow $P_{D(static)} + P_{D(dynamic)}$ to exceed $P_{D(max)}$, below.

where:

$P_{D(max)}$ = maximum power dissipation (dynamic + static power) (W)

150 = absolute maximum junction temperature (°C)

T_A = ambient temperature (°C) [68°F = 20°C]

Θ_{JA} = Junction thermal resistance:

63°C/W for SOIC package

40°C/W for SOIC with ePAD package

High-Frequency Operation

Although the MIC4478/4479/4480 drivers will operate at frequencies greater than 1MHz, the MOSFET's capacitance and the load will affect the output waveform (at the MOSFET's drain).

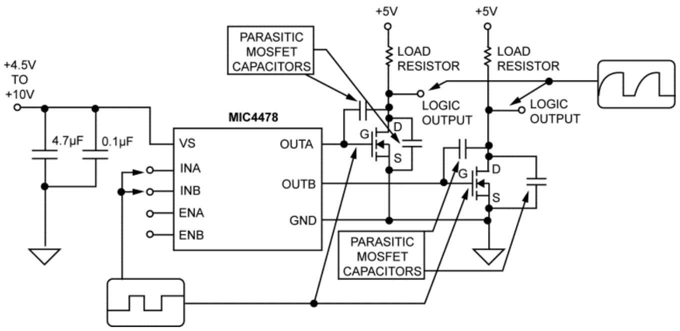
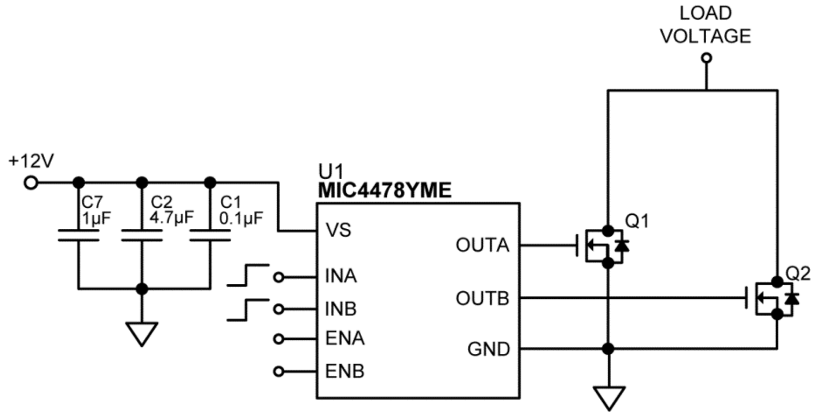


Figure 7. MOSFET Capacitance Effects at High Switching Frequency

When the MOSFET is driven off, slower rising occurs because the MOSFET's output capacitance recharges through the load resistance (RC circuit). A lower load resistance allows the output to rise faster. For the fastest driver operation, choose the smallest power MOSFET that will safely handle the desired voltage, current, and safety margin. The smallest MOSFETs generally have the lowest capacitance.

Typical Application Schematic



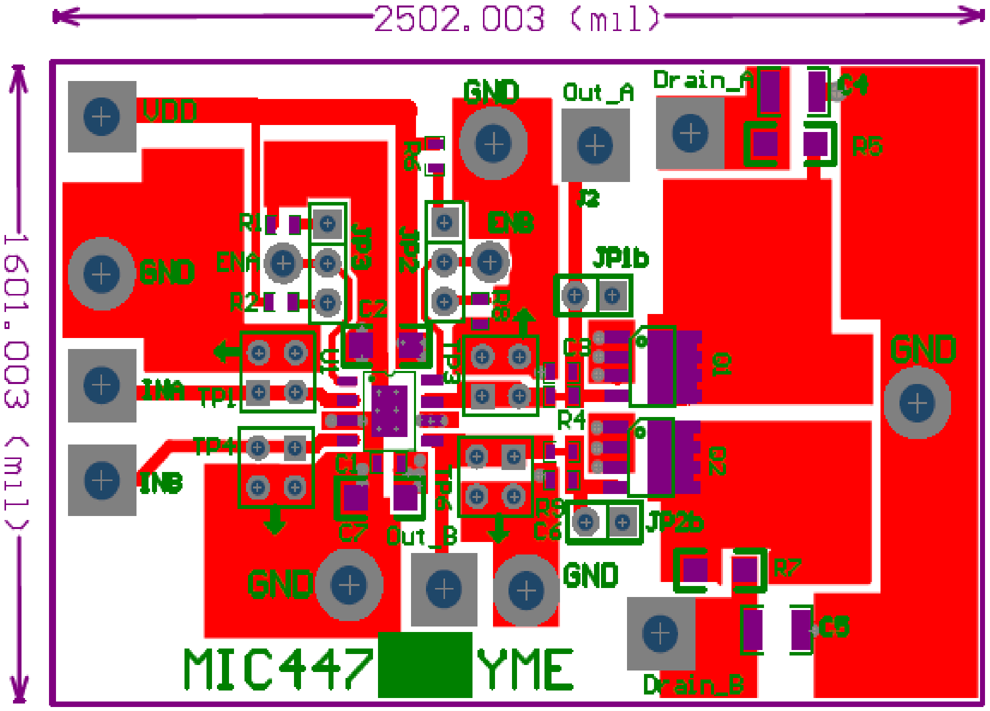
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	C1608X7R1H104K080AA	TDK(5)	0.1µF Ceramic Capacitor, 50V, X7R, Size 0603	1
C2	CGA4J3X5R1H475K125AB	TDK	4.7µF MLCC, 50V, X5R, Size 0805	1
C7	C3126X5R1H105K160AA	TDK	1µF Ceramic Capacitor, 50V, X5R, Size 1206	1
Q1, Q2	AM4492N	Analog Power(6)	100V, N-Channel MOSFET, SOIC-8	2
U1	**MIC4478YME**	**Micrel, Inc.**(7)	**32V Low-Side Dual MOSFET Driver**	1

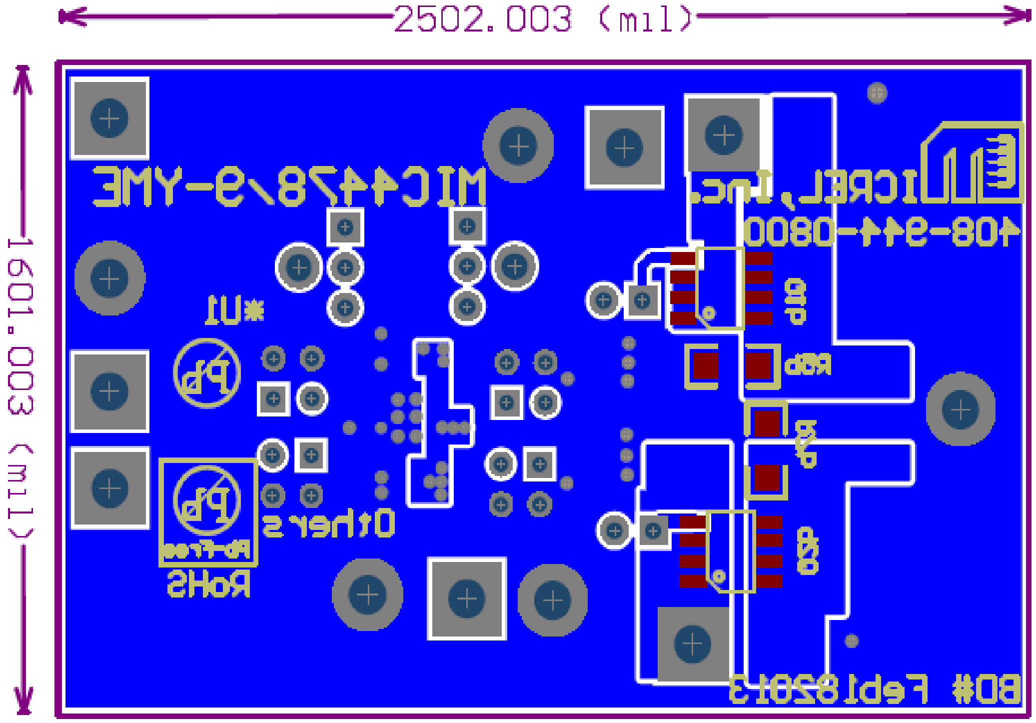
Notes:

5. TDK, Inc.: www.tdk.com.
6. Analog Power: www.analogpowerinc.com.
7. **Micrel, Inc.: www.micrel.com**.

PCB Layout Recommendations

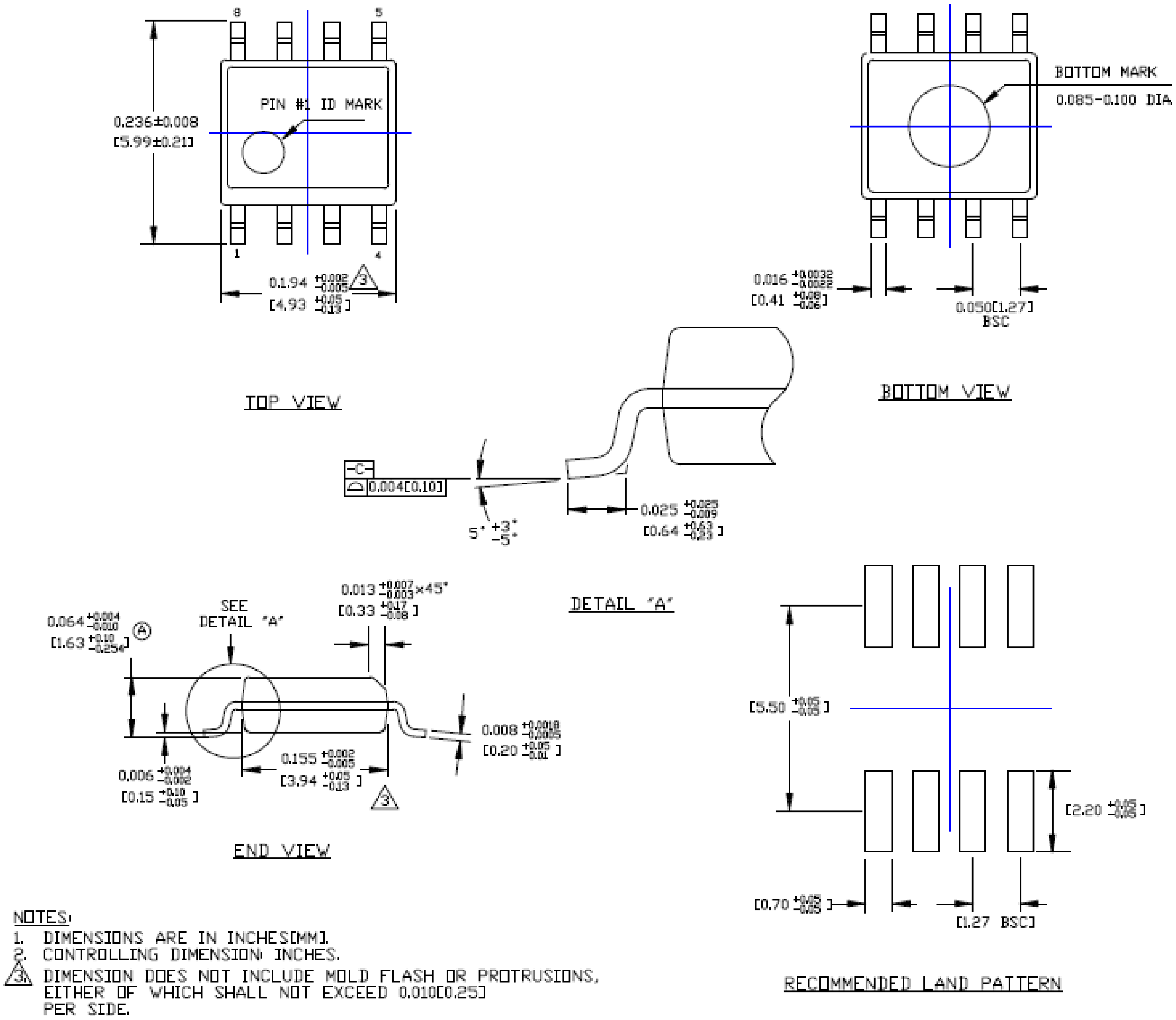


Top Layer



Bottom Layer

Package Information[8] and Recommended Land Pattern (8-pin SOIC)



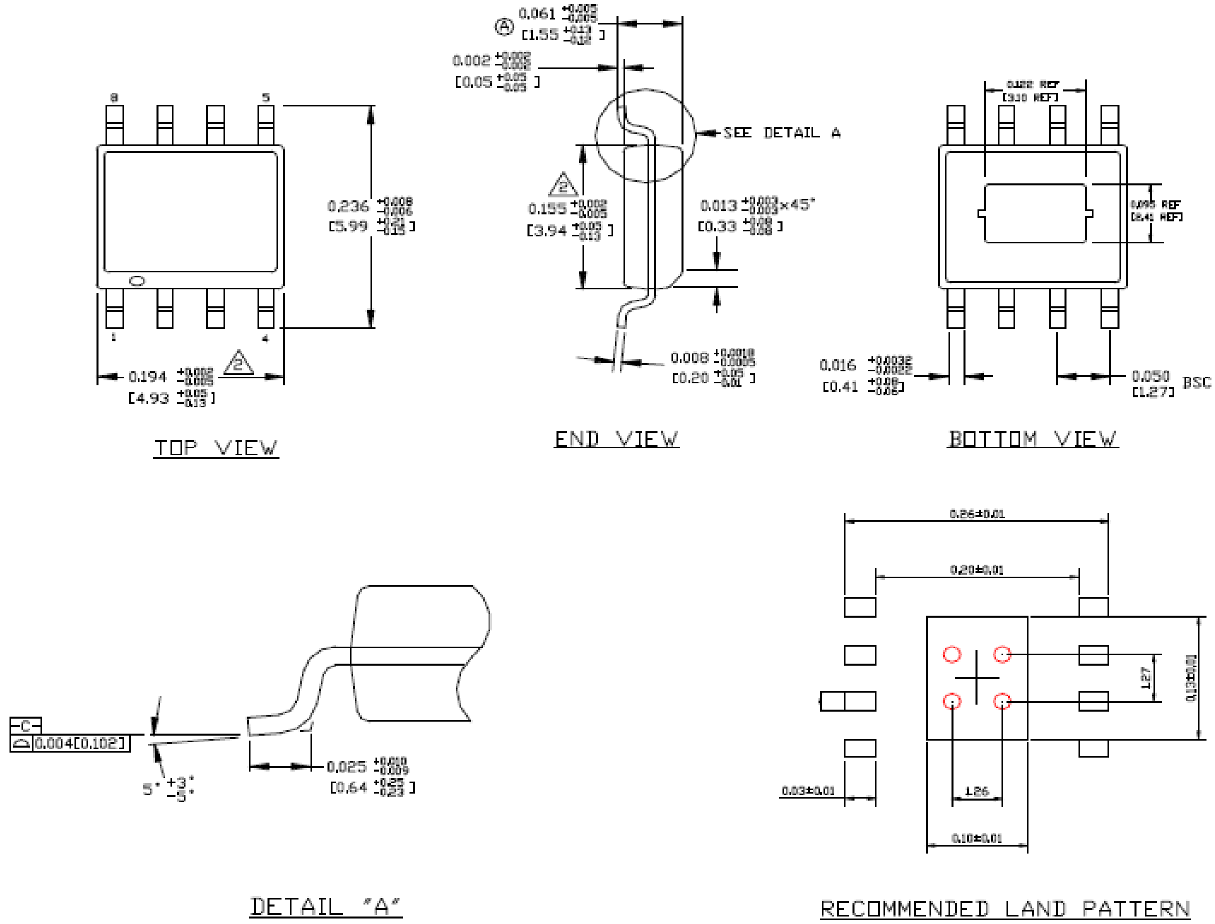
NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

8-Pin SOIC (M)

Note:

8. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Package Information[8] and Recommended Land Pattern (8-pin ePAD SOIC)



NOTE:

1. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL EXCEED 0.006 INCHES PER SIDE

2. RED CIRCLES IN LAND PATTERN REPRESENT THERMAL VIAS. RECOMMENDED SIZE IS 0.30-0.30MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAXIMUM THERMAL PERFORMANCE

8-Pin ePAD SOIC (ME)

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