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FUJITSU MICROELECTRONICS
DATA SHEET

DS04-27261-6E

ASSP for Power Management Applications of Ultra Mobile PC

6ch DC/DC Converter IC for LPIA Platform VR

MB39C308

■ DESCRIPTION

The MB39C308 is a 6ch DC/DC buck converter LSI, which integrates all of necessary power supplies for Ultra-Mobile PC powered by 2-cell Li-ion battery. And the MB39C308 uses current mode topology with N-channel synchronous rectification to realize high conversion efficiency.
The MB39C308 is the Power Management IC supporting the LPIA(Low Power Intel Architecture) which Intel Corporation proposes as the low power consumption platform for UMPC.

The CH1 and CH2 are flexible to adopt the output current capability by selection of external FETs and easy to optimize efficiency. The CH3, CH4, CH5 and CH6 integrate the switching FETs capable of high current for down-sizing the power supply solution.

The MB39C308 uses Fujitsu's LDMOS process technology and supplies all power without dispersing power from a lithium-ion battery.

■ FEATURES

- Input voltage range : 5.5 V to 12.6 V
- Topology : Current Mode
- Integrated FET Driver for external MOSFETs : CH1, CH2
- Integrated Switching MOSFETs : CH3, CH4, CH5, CH6
- Fixed Preset Output Voltage : CH1, CH2, CH5
- Selectable Preset Output Voltage : CH3, CH4, CH6

Channel	Output voltage	Output current	Remarks
CH1	5 V	2 A*	—
CH2	3.3 V	4.5 A*	—
CH3	1.8 V/1.5 V	Max : 2.7 A	DDR2/DDR3 are selectable.
CH4	0.9 V/0.75 V	Max : 1.5 A	
CH5	1.5 V	Max : 2.5 A	—
CH6	1.1 V/1.05 V	Max : 3.5 A	Two values are selectable.

* : It is the reference value at the typical EVB.

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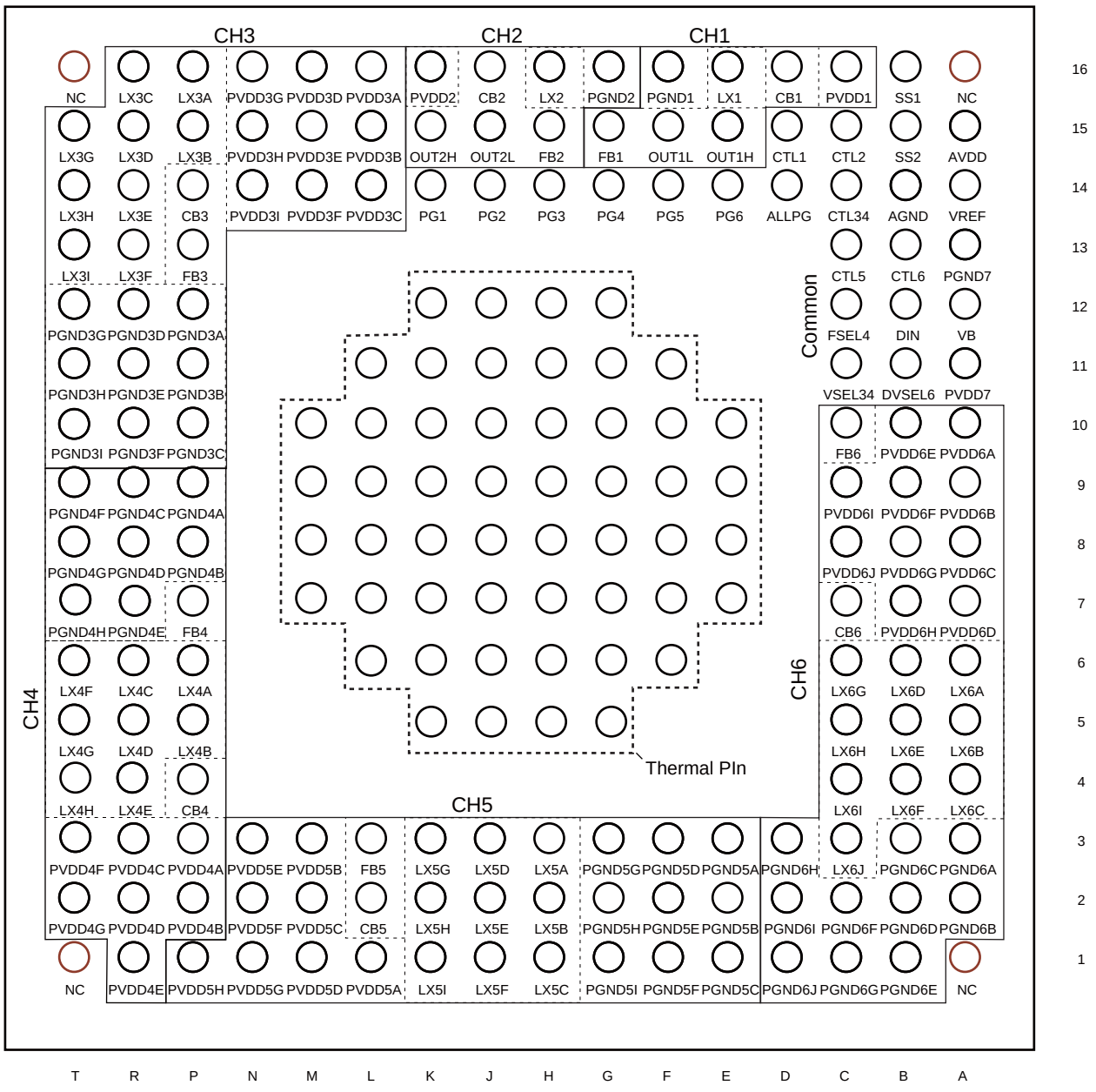
- PWM switching frequency : 0.7 MHz
  (CH4 : 0.7 MHz/0.35 MHz)
- Various protection
  - Over current protection (OCP)
  - Input over voltage protection (IVP)
  - Output short circuit protection (SCP)
  - Under voltage lock out protection (UVLO)
  - Output over voltage protection (OVP)
  - Over temperature protection (OTP)
- POWERGOOD function
- Soft start function independent from output loads.
- Soft stop function independent from output loads.
- High conversion efficiency in wide range of load current.
- Packaged in a compact package : PFBGA-208 (9.00 mm × 9.00 mm × 1.30 mm)

■ APPLICATIONS

- UMPC (Ultra Mobile PC)
- MID (Mobile Internet Device)
- Mobile equipment etc.

■ PIN ASSIGNMENT

(BOTTOM VIEW)



(BGA-208P-M02)(156-pin + Thermal 52-pin)

■ PIN DESCRIPTIONS

Block	Pin Name	I/O	Description
CH1	FB1	I	CH1 Error amplifier input pin, being connected to output of CH1.
	PVDD1	—	Power supply pin of the CH1 output block.
	CB1	O	Internal power supply pin of the CH1 gate driver block.
	LX1	—	CH1 inductor connection pin.
	OUT1H	O	CH1 High-side N-ch FET drive output pin.
	OUT1L	O	CH1 Low-side N-ch FET drive output pin.
	PGND1	—	Ground pin of the CH1 output block.
CH2	FB2	I	CH2 Error amplifier input pin, being connected to output of CH2.
	PVDD2	—	Power supply pin of the CH2 output block.
	CB2	O	Internal power supply pin of the CH2 gate driver block.
	LX2	—	CH2 inductor connection pin.
	OUT2H	O	CH2 High-side N-ch FET drive output pin.
	OUT2L	O	CH2 Low-side N-ch FET drive output pin.
	PGND2	—	Ground pin of the CH2 output block.
CH3	FB3	I	CH3 Error amplifier input pin, being connected to output of CH3.
	PVDD3A to PVDD3I	—	Power supply pins of the CH3 output block.
	CB3	O	Internal power supply pin of the CH3 gate driver block.
	LX3A to LX3I	—	CH3 inductor connection pins.
	PGND3A to PGND3I	—	Ground pins of the CH3 output block.
CH4	FB4	I	CH4 Error amplifier input pin, being connected to output of CH4.
	PVDD4A to PVDD4G	—	Power supply pins of the CH4 output block.
	CB4	O	Internal power supply pin of the CH4 gate driver block.
	LX4A to LX4H	—	CH4 inductor connection pins.
	PGND4A to PGND4H	—	Ground pins of the CH4 output block.

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Block	Pin Name	I/O	Description
CH5	FB5	I	CH5 Error amplifier input pin, being connected to output of CH5.
	PVDD5A to PVDD5H	—	Power supply pins of the CH5 output block.
	CB5	O	Internal power supply pin of the CH5 gate driver block.
	LX5A to LX5I	—	CH5 inductor connection pins.
	PGND5A to PGND5I	—	Ground pins of the CH5 output block.
CH6	FB6	I	CH6 Error amplifier input pin, being connected to output of CH6.
	PVDD6A to PVDD6J	—	Power supply pins of the CH6 output block.
	CB6	O	Internal power supply pin of the CH6 gate driver block.
	LX6A to LX6J	—	CH6 inductor connection pins.
	PGND6A to PGND6J	—	Ground pins of the CH6 output block.
Common	CTL1	I	CH1 Control input pin. (L : Standby / H : Normal operation)
	CTL2	I	CH2 Control input pin. (L : Standby / H : Normal operation)
	CTL34	I	CH3 and CH4 control input pin. (L : Standby / H : Normal operation)
	CTL5	I	CH5 Control input pin. (L : Standby / H : Normal operation)
	CTL6	I	CH6 Control input pin. (L : Standby / H : Normal operation)
	PG1	O	CH1 POWERGOOD output pin. (N-ch MOS open drain output)
	PG2	O	CH2 POWERGOOD output pin. (N-ch MOS open drain output)
	PG3	O	CH3 POWERGOOD output pin. (N-ch MOS open drain output)
	PG4	O	CH4 POWERGOOD output pin. (N-ch MOS open drain output)
	PG5	O	CH5 POWERGOOD output pin. (N-ch MOS open drain output)
	PG6	O	CH6 POWERGOOD output pin. (N-ch MOS open drain output)
	ALLPG	O	POWERGOOD output pin (The ALLPG pin outputs “H”, When channels CH3, CH4, CH5 and CH6 are the power good).
	FSEL4	I	CH4 switching frequency setting pin. FSEL4 = “H” : 700 kHz FSEL4 = “L” : 0.35 MHz (Shown in the “■ ELECTRICAL CHARACTERISTICS”)

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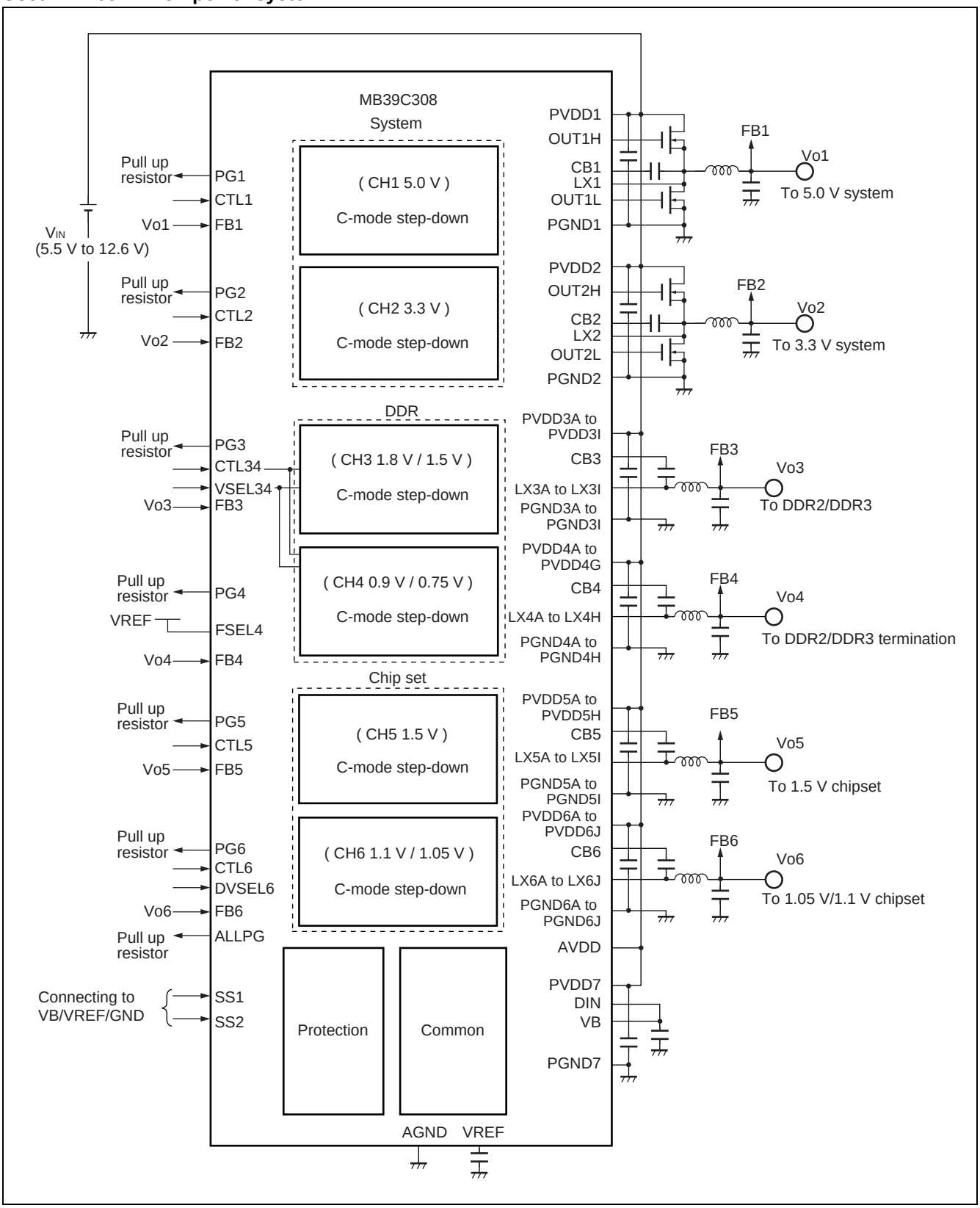
Block	Pin Name	I/O	Description
Common	VSEL34	I	Preset output voltage setting pin for CH3/CH4. VSEL34 = "H" : Vout_CH3 =1.8 V, Vout_CH4 = 0.9 V VSEL34 = "L" : Vout_CH3 =1.5 V, Vout_CH4 = 0.75 V
	DVSEL6	I	Preset output voltage setting pin for CH6 dynamically. DVSEL6 = "H" : Vout_CH6 = 1.1 V DVSEL6 = "L" : Vout_CH6 = 1.05 V
	SS1	I	Soft-Start and Soft-Stop time setting pin (Shown in the "■ DESCRIPTION OF SOFT-START AND SOFT-STOP OPERATION • Soft-Start/Soft-Stop time (tson/tsoff) Setting Conditions").
	SS2		
	VB	O	Bias voltage output pin for bootstrap and low-side N-ch gate driver of all channels.
	DIN	I	Bias voltage input pin for bootstrap. DIN pin should be connected with VB pin. (Shown in the "■ BLOCK DIAGRAM")
	PVDD7	—	Power supply pin of VB block.
	PGND7	—	Ground pin of VB block.
	AVDD	—	Power supply pin for common block.
	VREF	O	Reference voltage output pin.
	AGND	—	Ground pin of common block.

■ BLOCK DIAGRAM

Used in 2-cell Li-Ion power system



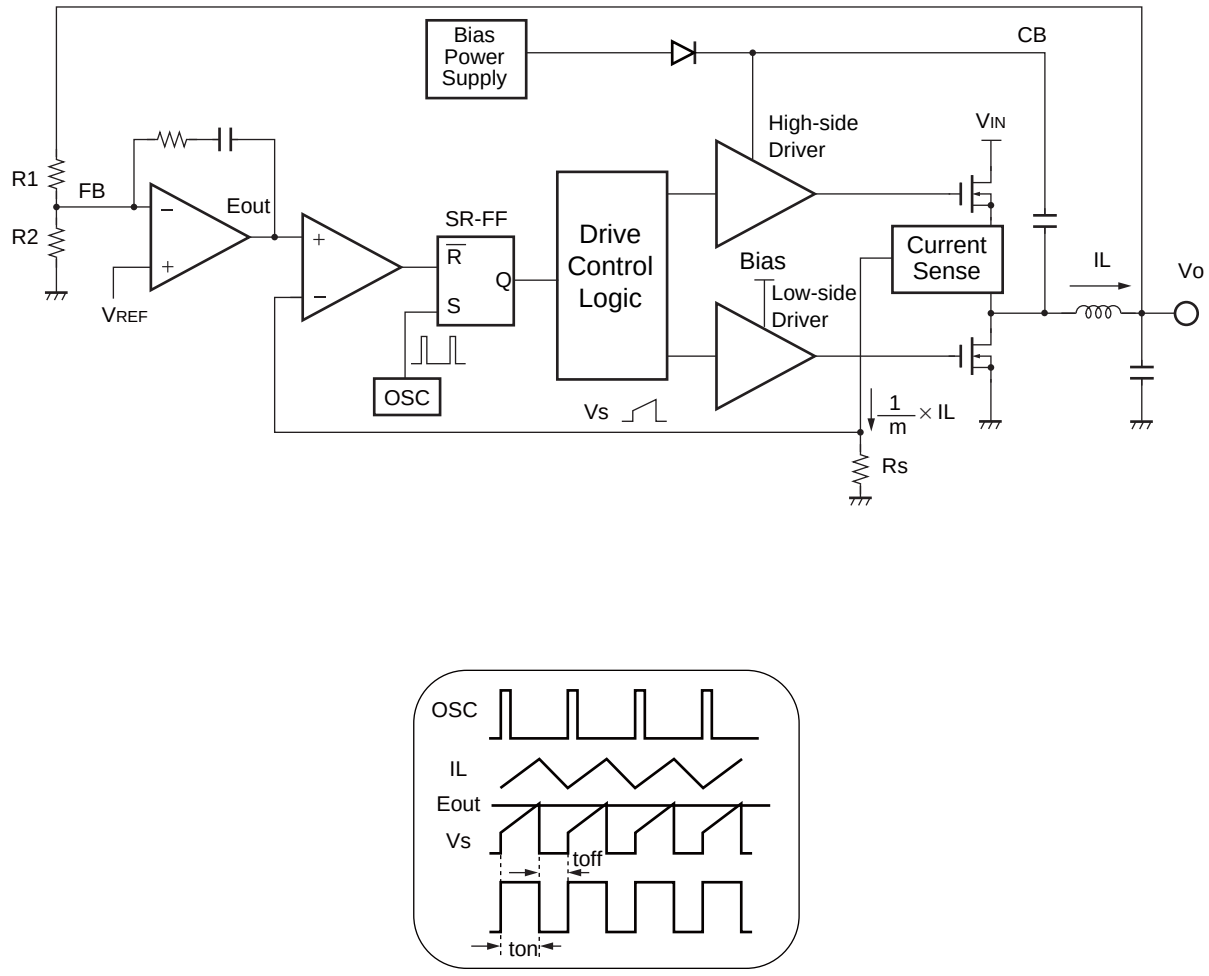
CURRENT MODE TOPOLOGY

A DC/DC regulation block of Current-mode (C-mode) is illustrated in the "• DC/DC topology, Current mode operation".

In this C-mode, the High-side FET is turned ON while the SR-FF is set at every clock cycle generated by on chip oscillator. During ON period (ton), the current is supplied by V_{IN}, then Inductor current(IL) is increased. Besides a current (IL/m), which senses the inductor current(IL), flows across a resistor (Rs) then the resister voltage (Vs) is increased. When the Vs reaches Eout , which is an output of the Error amp, the SR-FF is reset and the High-side FET is turned OFF (toff) until the next rising clock comes.

The voltage regulation is done by controlling a peak current of the inductor current (IL).

• DC/DC topology, Current mode operation



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{DD}	AVDD, PVDD1 to PVDD7 pin	–0.3	+ 13.5	V
CB voltage	V_{CB}	CB1 to CB6 pin	–0.3	+ 18.5	V
LX voltage	V_{LX}	LX1 to LX6 pin	–0.3	V_{DD}	V
CB to LX voltage	V_{CBLX}	CB pin to LX pin	–0.3	+ 7	V
OUTH voltage	V_{OUTH}	OUT1H, OUT2H pin	V_{LX} – 0.3	V_{CB}	V
OUTL voltage	V_{OUTL}	OUT1L, OUT2L pin	–0.3	+ 7	V
DIN voltage	V_{DIN}	DIN pin	–0.3	+ 7	V
VB voltage	V_{VB}	VB pin	–0.3	+ 7	V
VREF voltage	V_{VREF}	VREF pin	–0.3	+ 7	V
CTL voltage	V_{CTL}	CTL1 to CTL6 pin	–0.3	+ 13.5	V
VSEL voltage	V_{SEL}	VSEL34, DVSEL6 pin	–0.3	+ 7	V
FSEL voltage	V_{FSEL}	FSEL4 pin	–0.3	+ 7	V
FB voltage	V_{FB}	FB1 to FB6 pin	–0.3	+ 7	V
PG voltage	V_{PG}	PG1 to PG6, ALLPG pin	–0.3	+ 7	V
SS voltage	V_{SS}	—	–0.3	+ 7	V
Package power dissipation	P_D	Ta ≤ + 25 °C	—	2940*	mW
		Ta = + 85 °C	—	1180*	mW
Operating ambient temperature	Ta	—	–40	+ 85	°C
Storage temperature	T_{STG}	—	–55	+ 125	°C

* : See the diagram of "■ TYPICAL CHARACTERISTICS • Maximum Power Dissipation vs. Operating Ambient Temperature", for the package power dissipation of Ta from + 25 °C to + 85 °C.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

WARNING: The use of negative voltage below –0.3 Volts on the GND pins (AGND, PGND1 to PGND7) may activate parasitic transistors on the silicon, which can introduce abnormal operation.
Connecting the LX pin to either VDD pins (AVDD, PVDD1 to PVDD7) or GND pins (AGND, PGND1 to PGND7) directly may cause permanently damage to the device.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{DD}	AVDD = PVDD1 to PVDD7 pin	5.5	—	12.6	V
Input capacitor	C_{IN}	VDD to GND pin	—	4.7	—	µF
CB to LX capacitor	C_{CB}	CB to LX pin	—	0.1	—	µF
LX inductor	L1	LX1 pin	—	3.3	—	µH
	L2	LX2 pin	—	3.3	—	µH
	L3	LX3 pin	—	1.5	—	µH
	L4	LX4 pin, FSEL4 pin = H fosc = 0.7 MHz	—	1.5	—	µH
		LX4 pin, FSEL4 pin = L fosc = 0.35 MHz	—	1.5	—	
	L5	LX5 pin	—	1.5	—	µH
	L6	LX6 pin	—	1.5	—	µH
Output current	I_O1	Vo1 (5 V), DC, when Ron_{H1} = 32 mΩ	—	1	2*	A
	I_O2	Vo2 (3.3 V), DC, when Ron_{H2} = 16 mΩ	—	2.25	4.5*	A
	I_O3	Vo3 (1.8 V/1.5 V), DC	—	1.35	2.7*	A
	I_O4	Vo4 (0.9 V/0.75 V), DC	—	1	1.5*	A
	I_O5	Vo5 (1.5 V), DC	—	1.25	2.5*	A
	I_O6	Vo6 (1.1 V/1.05 V), DC	—	1.75	3.5*	A
Output capacitor	C_O1	Vo1 (5 V), when Ron_{H1} = 32 mΩ, L = 3.3 µH, SS1,SS2 pin = GND	—	100	300	µF
	C_O2	Vo2 (3.3 V), when Ron_{H1} = 16 mΩ, L = 3.3 µH, SS1,SS2 pin = GND	—	100	700	µF
	C_O3	Vo3 (1.8 V), when L = 1.5 µH, SS1, SS2 pin = GND	—	100	300	µF
	C_O4	Vo4 (0.9 V), when L = 1.5 µH, SS1, SS2 pin = GND	—	100	500	µF
	C_O5	Vo5 (1.5 V), when L = 1.5 µH, SS1, SS2 pin = GND	—	100	300	µF
	C_O6	Vo6 (1.05 V), when L = 1.5 µH, SS1, SS2 pin = GND	—	200	500	µF
External FET On-resistance	R_{onH1}	CH1 High-side FET connected to OUT1H pin	—	32	—	mΩ
	R_{onL1}	CH1 Low-side FET connected to OUT1L pin	—	32	—	mΩ
	R_{onH2}	CH2 High-side FET connected to OUT2H pin	12	16	20	mΩ
	R_{onL2}	CH2 Low-side FET connected to OUT2L pin	—	16	—	mΩ

(Continued)

(Continued)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
VB output capacitor	C_{VB}	VB pin	—	1	—	µF
VREF output capacitor	C_{VREF}	VREF pin	—	4.7	—	µF
VREF output current	I_{VREF}	VREF pin	– 1	—	0	mA
PG input voltage	V_{PG}	PG1 to PG6, ALLPG pin	—	—	6	V
PG sink current	I_{PG}	PG1 to PG6, ALLPG pin	—	—	2	mA
CTL input voltage	V_{CTL}	CTL1 to CTL6 pin	—	—	AVDD	V
VSEL input voltage	V_{SEL}	VSEL34, DVSEL6 pin	—	—	6	V
FSEL input voltage	V_{FSEL}	FSEL4 pin	—	—	6	V
SS input voltage	V_{SS}	SS1, SS2 pin	—	—	V_B	V

* : The MB39C308 is designed with assumed operating conditions, which is 60% of the maximum output current on the each channel and being operated with recommended input voltage range.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Ta = + 25 °C, AVDD = PVDD1 to PVDD7 = 7.2 V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Reference voltage block [VREF]	Reference voltage	V_{REF}	VREF pin = 0 mA	2.45	2.5	2.55	V
	Line regulation	VREF Line	AVDD pin = 5.5 V to 12.6 V	−10	—	+ 10	mV
	Load regulation	VREF Load	VREF pin = 0 mA to −1 mA	−15	—	+ 15	mV
Bias voltage block [VB]	Bias voltage	V_{VB}	5.5 V ≤ AVDD ≤ 12.6 V VB pin = 0 mA	4.8	5	5.2	V
	Load regulation	VB Load	VB pin = 0 mA to −1 mA	−15	—	+ 15	mV
Under-voltage lockout protection circuit block [UVLO]	Threshold voltage	V_{TLH}	AVDD pin	4.5	5.0	5.2	V
	Hysteresis width	V_{HU}	AVDD pin	0.05	0.1	0.4	V
Over-temperature protection circuit block [OTP]	Shutdown temperature	T_{OTPH}		—	+ 150*1	—	°C
	Hysteresis width	T_H		—	+ 25*1	—	°C
Input over voltage protection circuit block [IVP]	Threshold voltage	V_{IVPH}	AVDD pin	12.6	13.0	13.4	V
	Release voltage	V_{IVPL}	AVDD pin	12.5	12.85	13.3	V
	Hysteresis width	V_{HI}	AVDD pin	—	0.15	—	V
Oscillator block [OSC]	Oscillation frequency*2	fosc	CH1 to CH3, CH5, CH6 CH4 : FSEL4 pin = “H” Level	0.56	0.7	0.84	MHz
			CH4 : FSEL4 pin = “L” Level	0.28	0.35	0.42	MHz
Control block [CTL1 to CTL6]	Output on level	V_{IH}	CTL1 to CTL6 pin	2	—	—	V
	Output off level	V_{IL}	CTL1 to CTL6 pin	—	—	0.8	V
	Input current	I_{CTLH}	CTL1 to CTL6 pin = 3 V	23	30	43	µA
		I_{CTLL}	CTL1 to CTL6 pin = 0 V	—	—	1	µA

(Continued)

(Ta = + 25 °C, AVDD = PVDD1 to PVDD7 = 7.2 V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Output voltage select block [VSEL34, DVSEL6]	VSEL34, “H” level	V_{LGH}	VSEL34, DVSEL6 pin	2	—	—	V
	VSEL34, “L” level	V_{LGL}	VSEL34, DVSEL6 pin	—	—	0.8	V
	Input current	I_{SELH}	VSEL34, DVSEL6 pin = 3 V	23	30	43	µA
		I_{SELL}	VSEL34, DVSEL6 pin = 0 V	—	—	1	µA
Power good detection circuit block [PG1 to PG6, ALLPG]	Low side threshold voltage	V_{PGL}	FB1 to FB6 pin ↓ PG1 to PG6 pin	Vo × 0.85	Vo × 0.9	Vo × 0.95	V
	High side threshold voltage	V_{PGH}	FB1 to FB6 pin ↑ PG1 to PG6 pin	Vo × 1.05	Vo × 1.1	Vo × 1.15	V
	Hysteresis width	V_H	—	—	Vo × 0.03	—	V
	PG output low voltage	V_{OL}	PG1 to PG6, ALLPG pin = 1 mA	—	0.1	0.3	V
	PG leak current	I_{LKPG}	PG1 to PG6, ALLPG pin = 6 V	—	—	1	µA
Common block	AVDD standby current	I_{AVDDS}	CTL1 to CTL6 pin = 0 V, AVDD pin = 12.6 V	—	—	1	µA
	AVDD power supply current	I_{AVDD}	CTL1 to CTL6 pin = 3 V	—	0.25	—	mA
CH1 block [CH1]	CH1 output voltage	Vo1	FB1 pin	4.75	5	5.25	V
	PVDD1 standby current	I_{PVDD1S}	CTL1 pin = 0 V, PVDD1 pin = 12.6 V	—	—	15	µA
	CH1 efficiency	ηL1	0.05 × Io (Max) < Io < 0.3 × Io (Max)	87*3	—	—	%
		ηT1	0.3 × Io (Max) < Io < 0.6 × Io (Max)	92*3	—	—	%
		ηF1	0.6 × Io (Max) < Io< Io (Max)	92*3	—	—	%
	OUT1H source current	IsourceH1	Duty ≤ 5%, CB1 pin = 5 V, LX1 pin = 0 V, OUT1H pin = 0 V	—	–400*1	—	mA
	OUT1H sink current	IsinkH1	Duty ≤ 5%, CB1 pin = 5 V, LX1 pin = 0 V, OUT1H pin = 5 V	—	400*1	—	mA
	OUT1L source current	IsourceN1	Duty ≤ 5%, VB pin = 5 V, LX1 pin = 0 V, OUT1L pin = 0 V	—	–400*1	—	mA

(Continued)

(Ta = + 25 °C, AVDD = PVDD1 to PVDD7 = 7.2 V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
CH1 block [CH1]	OUT1L sink current	IsinkN1	Duty ≤ 5%, VB pin = 5 V, LX1 pin = 0 V, OUT1L pin = 5 V	—	400*1	—	mA
	OUT1H on resistance	R_{OH1}	OUT1H pin = –15 mA	—	12	18	Ω
		R_{OL1}	OUT1H pin = 15 mA	—	12	18	Ω
	OUT1L on resistance	R_{OH1}	OUT1L pin = –15 mA	—	12	18	Ω
		R_{OL1}	OUT1L pin = 15 mA	—	12	18	Ω
	Vo1 output over voltage threshold	Vo1	FB1 pin	5.9*1	6*1	6.1*1	V
	Vo1 over current limit	I_{OCP1}	Io1 Ron_{H1} = 32 mΩ, L = 3.3 µH	3.4*1	4.0*1	4.6*1	A
	FB1 input resistance	R_{FB1}	FB1 pin	—	340	—	kΩ
	Soft Start time	SS1	FB1 pin SS1 = SS2 = AGND pin	1.19	1.4	1.61	ms
CH2 block [CH2]	CH2 output voltage	Vo2	FB2 pin	3.135	3.3	3.465	V
	PVDD2 standby current	I_{PVDD2S}	CTL2 pin = 0 V, PVDD2 pin = 12.6 V	—	—	15	µA
	CH2 efficiency	ηL2	0.05 × Io (Max) < Io < 0.3 × Io (Max)	87*3	—	—	%
		ηT2	0.3 × Io (Max) < Io < 0.6 × Io (Max)	92*3	—	—	%
		ηF2	0.6 × Io (Max) < Io < Io (Max)	92*3	—	—	%
	OUT2H source current	IsourceH2	Duty ≤ 5%, CB2 pin = 5 V, LX2 pin = 0 V, OUT2H pin = 0 V	—	– 400	—	mA
	OUT2H sink current	IsinkH2	Duty ≤ 5%, CB2 pin = 5 V, LX2 pin = 0 V, OUT2H pin = 5 V	—	400	—	mA
	OUT2L source current	IsourceN2	Duty ≤ 5%, VB pin = 5 V, LX2 pin = 0 V, OUT2L pin = 0 V	—	– 400	—	mA
	OUT2L sink current	IsinkN2	Duty ≤ 5%, VB pin = 5 V, LX2 pin = 0 V, OUT2L pin = 5 V	—	400	—	mA
	OUT2H on resistance	R_{OH2}	OUT2H pin = –15 mA	—	12	18	Ω
		R_{OL2}	OUT2H pin = 15 mA	—	12	18	Ω
	OUT2L on resistance	R_{OH2}	OUT2L pin = –15 mA	—	12	18	Ω
		R_{OL2}	OUT2L pin = 15 mA	—	12	18	Ω

(Continued)

(Ta = + 25 °C, AVDD = PVDD1 to PVDD7 = 7.2 V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
CH2 block [CH2]	Vo2 output over voltage threshold	Vo2	FB2 pin	3.894*1	3.96*1	4.026*1	V
	Vo2 over current limit	I_{OCP2}	I_O2 Ron_{H1} = 16 mΩ, L = 3.3 μH	6.7*1	7.9*1	9.0*1	A
	FB2 input resistance	R_{FB2}	FB2 pin	—	220	—	kΩ
	Soft start time	SS2	FB2 pin SS1 = SS2 = AGND pin	1.19	1.4	1.61	ms
CH3 block [CH3]	CH3 output voltage	Vo3	VSEL34 = “H” Level, FB3 pin	1.71	1.8	1.89	V
			VSEL34 = “L” Level, FB3 pin	1.425	1.5	1.575	V
	High-side FET on-resistance	R_{ONH3}	LX3 pin = –100 mA, V_{GS} = 5 V	—	65*1	—	mΩ
	Low-side FET on-resistance	R_{ONL3}	LX3 pin = 100 mA, V_{GS} = 5 V	—	40*1	—	mΩ
	PVDD3 standby current	I_{PVDD3S}	CTL34 pin = 0 V, PVDD3 pin = 12.6 V	—	—	15	μA
	CH3 efficiency	ηL31	VSEL34 pin = “H” Level, Vo3 = 1.8 V 0.05 × Io (Max) < Io < 0.3 × Io (Max)	85*3	—	—	%
		ηL32	VSEL34 pin = “L” Level, Vo3 = 1.5 V 0.05 × Io (Max) < Io < 0.3 × Io (Max)	82*3	—	—	%
		ηT31	VSEL34 pin = “H” Level, Vo3 = 1.8 V 0.3 × Io (Max) < Io < 0.6 × Io (Max)	87*3	—	—	%
		ηT32	VSEL34 pin = “L” Level, Vo3 = 1.5 V 0.3 × Io (Max) < Io < 0.6 × Io (Max)	85*3	—	—	%
		ηF31	VSEL34 pin = “H” Level, Vo3 = 1.8 V 0.6 × Io (Max) < Io < Io (Max)	87*3	—	—	%
		ηF32	VSEL34 pin = “L” Level, Vo3 = 1.5 V 0.6 × Io (Max) < Io < Io (Max)	85*3	—	—	%

(Continued)

(Ta = + 25 °C, AVDD = PVDD1 to PVDD7 = 7.2 V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
CH3 block [CH3]	Vo3 output over voltage threshold	V_{OVP3}	VSEL34 pin = “H” Level, Vo3 = 1.8 V, FB3 pin	2.124*1	2.16*1	2.196*1	V
			VSEL34 pin = “L” Level, Vo3 = 1.5 V, FB3 pin	1.77*1	1.8*1	1.83*1	V
	Vo3 over current limit	I_{OCP3}	Io3, L = 1.5 µH	3.0*1	3.75*1	4.5*1	A
	FB3 input resistance	R_{FB3}	FB3 pin	—	250	—	kΩ
	Soft start time	SS3	FB3 pin SS1 = SS2 = AGND pin	1.19	1.4	1.61	ms
CH4 block [CH4]	CH4 output voltage	Vo4	VSEL34 pin = “H” Level, FB4 pin	0.855	0.9	0.945	V
			VSEL34 pin = “L” Level, FB4 pin	0.7125	0.75	0.7875	V
	High-side FET on-resistance	R_{ONH4}	LX4 pin = −100 mA, V_{GS} = 5 V	—	130*1	—	mΩ
	Low-side FET on-resistance	R_{ONL4}	LX4 pin = 100 mA, V_{GS} = 5 V	—	55*1	—	mΩ
	PVDD4 standby current	I_{PVDD4S}	CTL34 pin = 0 V, PVDD4 pin = 12.6 V	—	—	15	µA
	CH4 efficiency	ηT41	VSEL34 pin = “H” Level, FSEL4 pin =“H” Level, Vo4 = 0.9 V 0.3 × Io (Max) < Io < 0.6 × Io (Max)	80*3	—	—	%
		ηT42	VSEL34 pin = “L” Level, FSEL4 pin =“H” Level, Vo4 = 0.75 V 0.3 × Io (Max) < Io < 0.6 × Io (Max)	80*3	—	—	%
		ηF41	VSEL34 pin = “H” Level, FSEL4 pin =“H” Level, Vo4 = 0.9 V 0.6 × Io (Max) < Io < Io (Max)	83*3	—	—	%
		ηF42	VSEL34 pin = “L” Level, FSEL4 pin =“H” Level, Vo4 = 0.75 V 0.6 × Io (Max) < Io < Io (Max)	83*3	—	—	%
	Vo4 output over voltage threshold	V_{OVP4}	VSEL34 pin = “H” Level, Vo4 = 0.9 V, FB4 pin	1.035*1	1.08*1	1.125*1	V
			VSEL34 pin = “L” Level, Vo4 = 0.75 V, FB4 pin	0.862*1	0.90*1	0.938*1	V

(Continued)

(Ta = + 25 °C, AVDD = PVDD1 to PVDD7 = 7.2 V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
CH4 block [CH4]	Vo4 over current limit	I_{OCP4}	Io4, L = 1.5 µH,fosc = 700 kHz	1.92*1	2.4*1	2.88*1	A
	FB4 input resistance	R_{FB4}	FB4 pin	—	750	—	kΩ
	Soft start time	SS4	FB4 pin, SS1 = SS2 = AGND pin	1.19	1.4	1.61	ms
	FSEL4, “H” level	V_{FLGH4}	FSEL4 pin	2	—	—	V
	FSEL4, “L” level	V_{FLGL4}	FSEL4 pin	—	—	0.8	V
	FSEL4 input current	I_{FSELH4}	FSEL4 pin = 3 V	23	30	43	µA
		I_{FSELL4}	FSEL4 pin = 0 V	—	—	1	µA
CH5 block [CH5]	CH5 output voltage	Vo5	FB5 pin	1.425	1.5	1.575	V
	High-side FET on-resistance	R_{ONH5}	LX5 pin = –100 mA, V_{GS} = 5 V	—	65*1	—	mΩ
	Low-side FET on-resistance	R_{ONL5}	LX5 pin = 100 mA, V_{GS} = 5 V	—	40*1	—	mΩ
	PVDD5 standby current	I_{PVDD5S}	CTL5 pin = 0 V, PVDD5 pin = 12.6 V	—	—	15	µA
	CH5 efficiency	ηL5	0.05 × Io (Max) < Io < 0.3 × Io (Max)	82*3	—	—	%
		ηT5	0.3 × Io (Max) < Io < 0.6 × Io (Max)	85*3	—	—	%
		ηF5	0.6 × Io (Max) < Io < Io (Max)	85*3	—	—	%
	Vo5 output over voltage threshold	V_{OVP5}	FB5 pin	1.77*1	1.8*1	1.83*1	V
	Vo5 over current limit	I_{OCP5}	Io5, L = 1.5 µH	2.8*1	3.5*1	4.2*1	A
	FB5 input resistance	R_{FB5}	FB5 pin	—	250	—	kΩ
	Soft start time	SS5	FB5 pin, SS1 = SS2 = AGND pin	1.19	1.4	1.61	ms
CH6 block [CH6]	CH6 output voltage	Vo6	DVSEL6 = “H” Level, FB6 pin	1.045	1.1	1.155	V
			DVSEL6 = “L” Level, FB6 pin	0.9975	1.05	1.1025	V
	High-side FET on-resistance	R_{ONH6}	LX6 pin = –100 mA, V_{GS} = 5 V	—	61*1	—	mΩ
	Low-side FET on-resistance	R_{ONL6}	LX6 pin = 100 mA, V_{GS} = 5 V	—	35*1	—	mΩ
	PVDD6 standby current	I_{PVDD6S}	CTL6 pin = 0 V, PVDD6 pin = 12.6 V	—	—	15	µA

(Continued)

(Continued)

(Ta = + 25 °C, AVDD = PVDD1 to PVDD7 = 7.2 V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
CH6 block [CH6]	CH6 efficiency	ηL61	DVSEL6 pin = “H” Level, Vo6 = 1.1 V 0.05 × Io (Max) < Io < 0.3 × Io (Max)	80*3	—	—	%
		ηL62	DVSEL6 pin = “L” Level, Vo6 = 1.05 V 0.05 × Io (Max) < Io < 0.3 × Io (Max)	80*3	—	—	%
		ηT61	DVSEL6 pin = “H” Level, Vo6 = 1.1 V 0.3 × Io (Max) < Io < 0.6 × Io (Max)	82*3	—	—	%
		ηT62	DVSEL6 pin = “L” Level, Vo6 = 1.05 V 0.3 × Io (Max) < Io < 0.6 × Io (Max)	82*3	—	—	%
		ηF61	DVSEL6 pin = “H” Level, Vo6 = 1.1 V 0.6 × Io (Max) < Io < Io (Max)	81*3	—	—	%
		ηF62	DVSEL6 pin = “L” Level, Vo6 = 1.05 V 0.6 × Io (Max) < Io < Io (Max)	81*3	—	—	%
	Vo6 output over voltage threshold	V_{OVP6}	DVSEL6 pin = “H” Level, Vo6 = 1.1 V, FB6 pin	1.298*1	1.32*1	1.342*1	V
			DVSEL6 pin = “L” Level, Vo6 = 1.05 V, FB6 pin	1.239*1	1.26*1	1.281*1	V
	Vo6 over current limit	I_{OCP6}	Io6, L = 1.5 µH	4.0*1	5.0*1	6.0*1	A
	FB6 input resistance	R_{FB6}	FB6 pin	—	350	—	kΩ
	Soft start time	SS6	FB6 pin, SS1 = SS2 = AGND pin	1.19	1.4	1.61	ms

*1 : This parameter isn't be specified. This should be used as a reference to support designing the circuits.

*2 : FSEL4 pin is typically recommended to set to “H” level for fosc = 700 kHz setting. When Vo4 is preset to 0.75 V, the ON duty becomes so small at high input voltage. Then, there is a case CH4 output regulation becomes worse at light load condition. In that case, please set FSEL4 pin to “L” level for fosc = 350 kHz setting.

*3 : This is a reference value, which is evaluated by the recommended EVB circuit. This should be used as a reference to support designing the circuits.

■ CHANNEL CONTROL FUNCTION

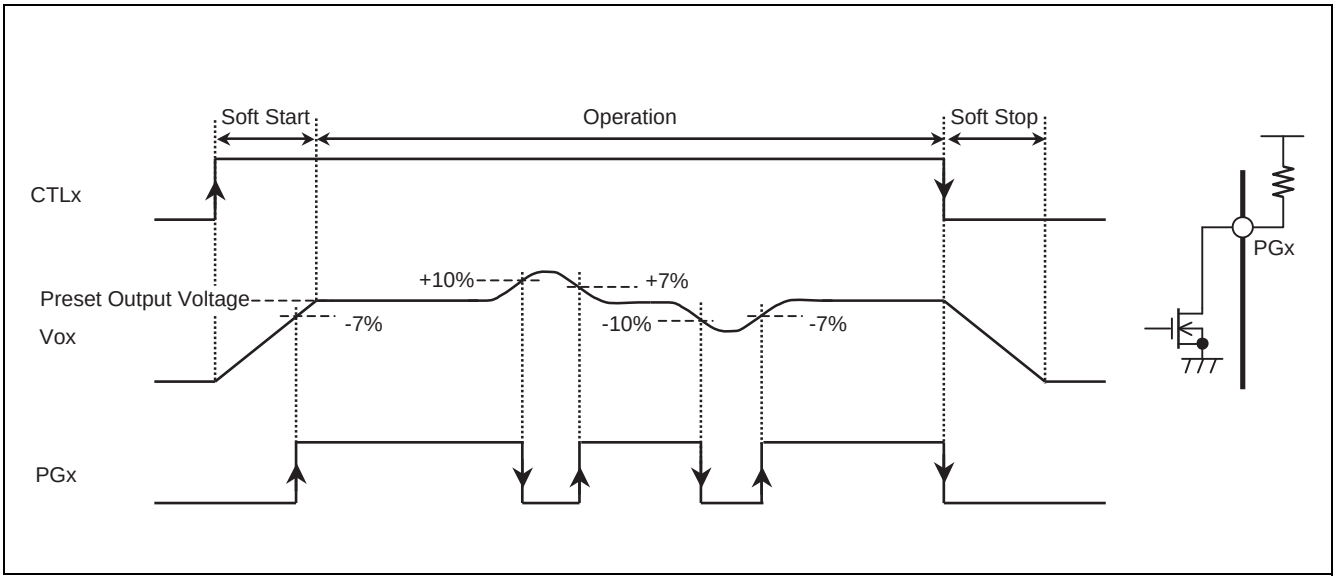
The each channel is turned on and off depending on the voltage levels at the CTL1 pin, CTL2 pin, CTL34 pin, CTL5 pin and CTL6 pin.

• Channel On/Off Setting Conditions

CTL1	CTL2	CTL34	CTL5	CTL6	CH1	CH2	CH3	CH4	CH5	CH6
L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF
H	L	L	L	L	ON	OFF	OFF	OFF	OFF	OFF
L	H	L	L	L	OFF	ON	OFF	OFF	OFF	OFF
L	L	H	L	L	OFF	OFF	ON	ON	OFF	OFF
L	L	L	H	L	OFF	OFF	OFF	OFF	ON	OFF
L	L	L	L	H	OFF	OFF	OFF	OFF	OFF	ON
H	H	H	H	H	ON	ON	ON	ON	ON	ON

■ POWER GOOD FUNCTION

The Power Good function is shown in the following figure. The ALLPG pin and the PGx pins are connected to the open drain of the NMOS, and are used by connecting the resistor. When the CTLx pin is turned on, and the output voltage becomes within 7% of the preset voltage, the PGx pin is changed from “L” to “H”. PGx = “H” means the status of Power Good. When the change of the output voltage exceeds 10% of the preset voltage, the PGx pin becomes “L”. And when the output voltage becomes within 7% of the preset voltage, the PGx pin becomes “H”. Moreover, when all of the channels from CH3 to CH6 are the Power Good, the ALLPG pin becomes “H”.



■ PROTECTION

<1> Under Voltage Lock Out Protection (UVLO)

The UVLO prevents IC malfunctions or system damage and the degradation caused by the excessive voltage or instantaneous voltage drop of the power supply voltage (AVDD), bias voltage (VB), internal reference voltage (VREF).
The UVLO turns off all the high- and low-side FETs of CH1 to CH6 when the AVDD pin drops below 5.0 V(Typ). The UVLO is released when the AVDD pin is above 5.1 V (Typ). This is the non-latch type protection.

<2> Input Over Voltage Protection (IVP)

The circuit prevents IC malfunctions or system damage and the degradation caused by the excessive voltage or instantaneous voltage drop of the power supply voltage (AVDD).
The IVP turns off all the high- and low-side FETs of CH1 to CH6 when the AVDD pin exceeds 13.0 V(Typ). The IVP is released when the AVDD pin drops below 12.85 V (Typ). This is the non-latch type protection.

<3> Over Temperature Protection (OTP)

The OTP prevents thermal damages on ICs. The IVP function turns off all the high- and low-side FETs of CH1 to CH6 when the junction temperature exceeds +150 °C (Typ). The OPT is released when the temperature drops below +125 °C (Typ). This is the non-latch type protection.

<4> Output Short Circuit Protection (SCP)

The SCP function stops outputting data when the output voltage falls and protects the devices connected to outputs.
The SCP timer will start to count when either of output voltages CH1 to CH6 falls due to the output short-circuit to GND or excessive currents. The SCP function starts to operate the latch protection and turns off all the high- and low-side FETs when the output voltage continues to fall to 1.4 ms (Typ).
Follow either of the steps to release the latch of output short circuit protection.

- After all of CTL signals from CH1 to CH6 are set to “L” level, turn on the each CTL signal again.
- When the voltage of the AVDD pin is below the threshold voltage of the UVLO, and then the voltage of the AVDD pin becomes higher than the threshold voltage of UVLO again, the each output will start up.

<5> Output Over Voltage Protection (OVP)

The OVP protects the devices which are connected to outputs when the output voltage rises. When either output voltage of the CH1 to CH6 is higher than 120% of each channel's preset voltage (Typ), the OVP turns off all the high- and low-side FETs of the channels (However, the only CH4 is turned off the high-side FET and turned on the low-side FET. The CH4 logic is different from other channels as it is controlled with PWM). The OVP is released when the output voltage is below 103% of the preset voltage (Typ). This is the non-latch type protection.

<6> Over Current Protection (OCP)

The OCP function controls the output current. When drain-to-source current excessively increases, the OCP controls the output current to the preset value for each channel. Then, because of the OCP functions, the output voltage usually drops. As a result, the SCP stop the all outputs with the latch setting.
The OCP functions only for the corresponding channels only, however, the SCP stops all of the channels in the end.

■ DESCRIPTION OF SOFT-START AND SOFT-STOP OPERATION

Soft-start function is featured to avoid inrush current when each channels is turned-on. When the CTL1, CTL2, CTL34, CTL5 and CTL6 are set to “H” level, ramped-up voltage is fed on an inverting input of an error amplifier of a channel. Start-time of the soft-start can be predefined and the start time is kept constant independent from a load of the output of the channels. When the CTL1, CTL2, CTL34, CTL5 and CTL6 are set to “L” level, ramped-down voltage is fed on an inverting input of an error amplifier of a channel then the output voltage goes low. Stop-time of the Soft-stop can be predefined and the stop-time is kept constant independent from a load of the output of the channel.

The time of both soft-start and soft-stop can be predefined with combination of the level on the SS1 and the SS2 pins as shown in the “• Soft-Start/Soft-Stop time (tson/tsoff) Setting Conditions”, and external capacitors and resistors aren't required

• Soft-Start/Soft-Stop time (tson/tsoff) Setting Conditions

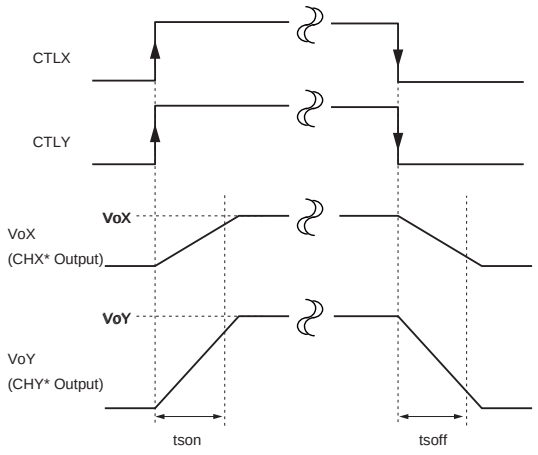
SS1 pin	SS2 pin	Soft-Start time (tson) (Typ) *	Soft-Stop time (tsoff) (Typ) *	Unit
Connecting to AGND pin	Connecting to AGND pin	1.4	1.4	ms
Connecting to AGND pin	Connecting to VREF pin	2.2	2.2	ms
Connecting to AGND pin	Connecting to VB pin	2.9	2.9	ms
Connecting to VREF pin	Connecting to AGND pin	3.5	3.5	ms
Connecting to VREF pin	Connecting to VREF pin	4.1	4.1	ms
Connecting to VREF pin	Connecting to VB pin	5.1	5.1	ms
Connecting to VB pin	Connecting to AGND pin	5.9	5.9	ms
Connecting to VB pin	Connecting to VREF pin	7.3	7.3	ms
Connecting to VB pin	Connecting to VB pin	8.2	8.2	ms

* : Accuracy : Typ ±15%

<< Trace of the Output voltage on each channel, during Soft-Start/Soft-Stop operations>>

The sequence of turning on/off different output channels is defined by the CTL1, CTL2, CTL34, CTL5 and CTL6 pins.

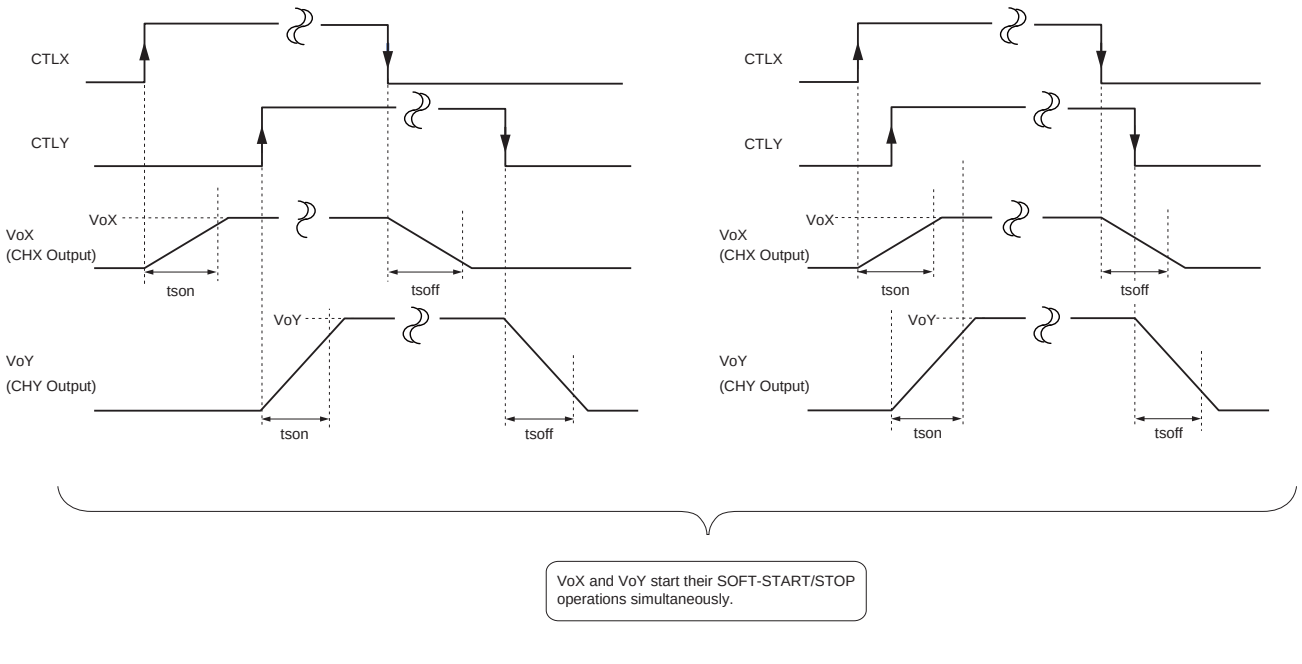
(1) When CTLX and CTLY are set to "H" or "L" simultaneously.



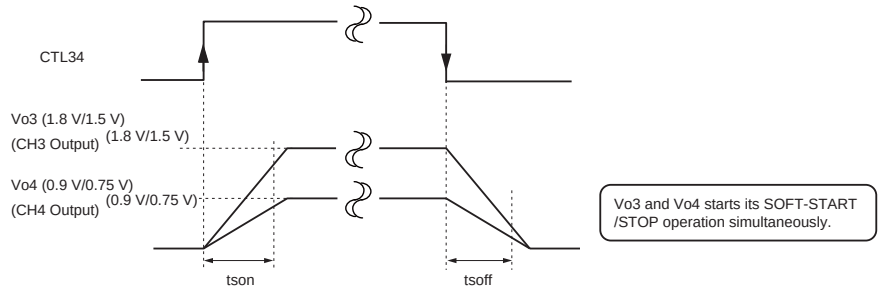
* : CHY and CHX are different CH.

(2) When CTLY is set to "H" or "L" after completion of SOFT-START or -STOP on VoX .

(3) When CTLY is set to "H" or "L" after VoX has started its SOFT-START or -STOP operation.



(4) When CTL34 is set to “H” or “L”.



■ PRESET FUNCTION OF CH3/CH4/CH6 OUTPUT VOLTAGE

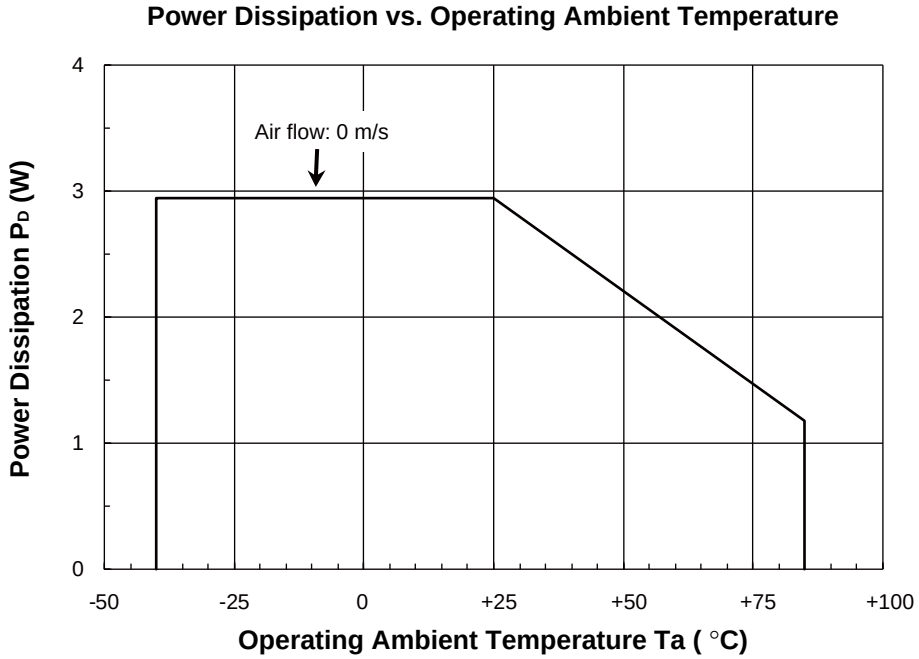
The preset output voltage of CH3 and CH4 are selected by VSEL34 pin condition. Please refer the following table. The preset output voltage of CH6 is selected by DVSEL6 pin condition. Please refer the following table.

- CH3/CH4/CH6 Preset Output Voltage Conditions

CONNECTION	VREF	GND
VSEL34	Vo3 = 1.8 V setting Vo4 = 0.9 V setting	Vo3 = 1.5 V setting Vo4 = 0.75 V setting
DVSEL6	Vo6 = 1.1 V setting	Vo6 = 1.05 V setting

■ TYPICAL CHARACTERISTICS

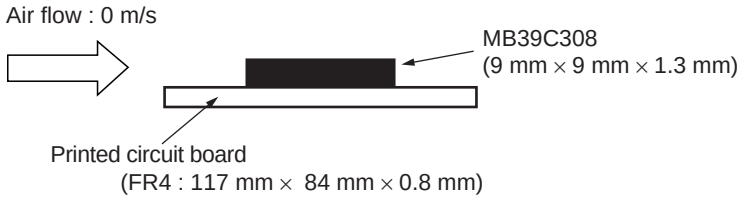
• Maximum Power Dissipation vs. Operating Ambient Temperature



The Allowable power dissipation is shown in the "• Maximum Power Dissipation vs. Operating Ambient Temperature". The maximum power dissipation depends on the thermal capability of the given package, and the ambient temperature.

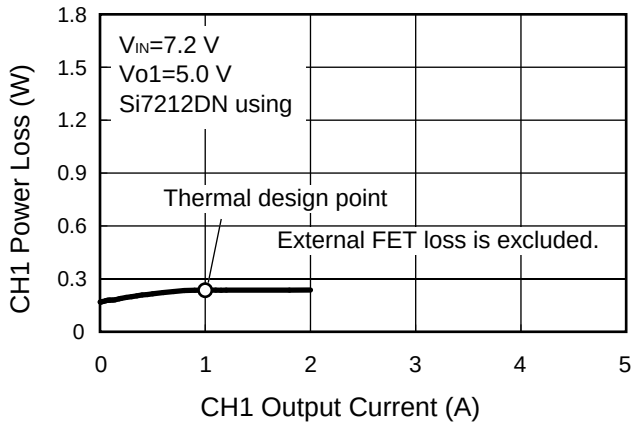
Sum of power dissipation of each channel (CH1 to CH6) should not exceed the maximum rating. Expected power loss of the each channel's over load current are shown in the "• Power Loss Curve for each channel".

• The condition of the thermal model

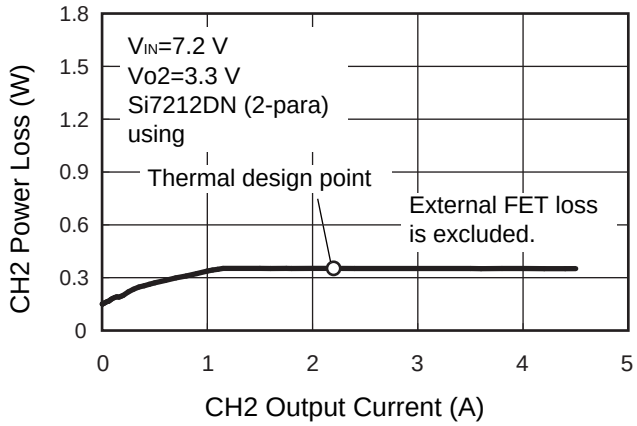


• Power Loss Curve for each channel

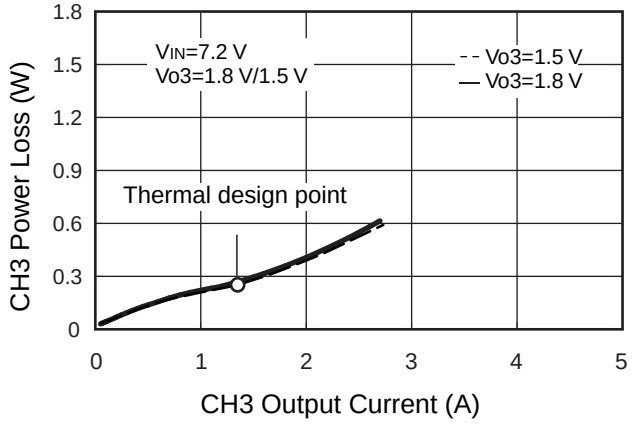
CH1 Output Current vs. Power Loss



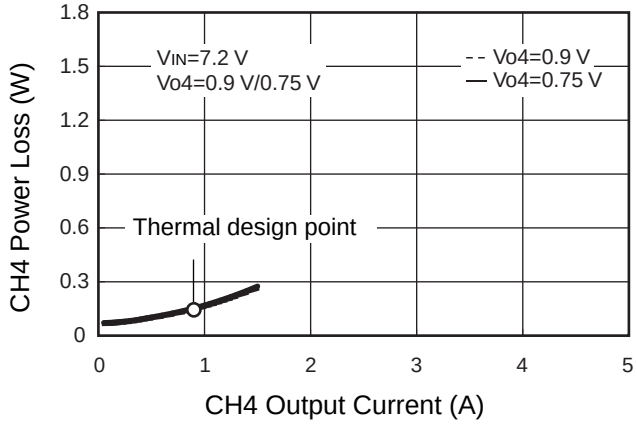
CH2 Output Current vs. Power Loss



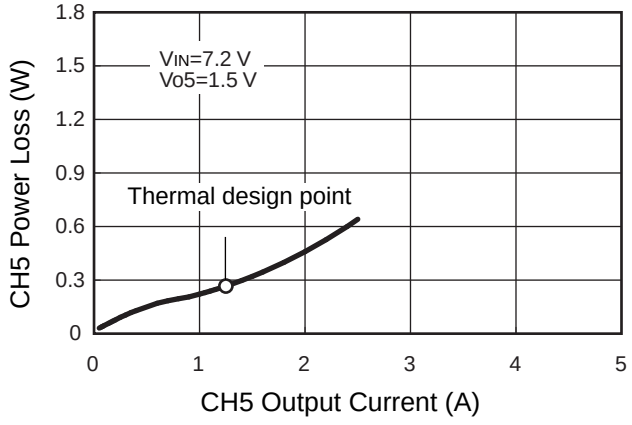
CH3 Output Current vs. Power Loss



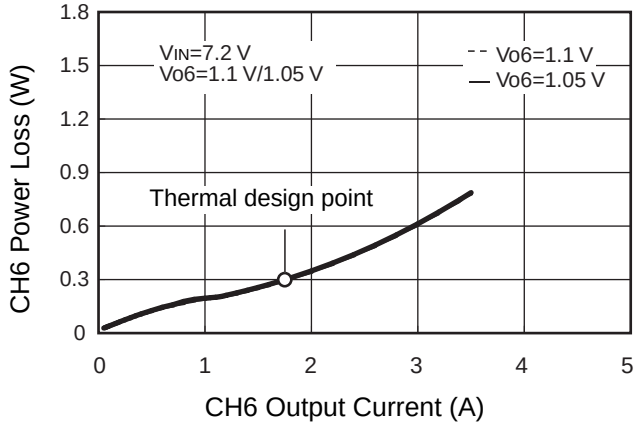
CH4 Output Current vs. Power Loss



CH5 Output Current vs. Power Loss



CH6 Output Current vs. Power Loss

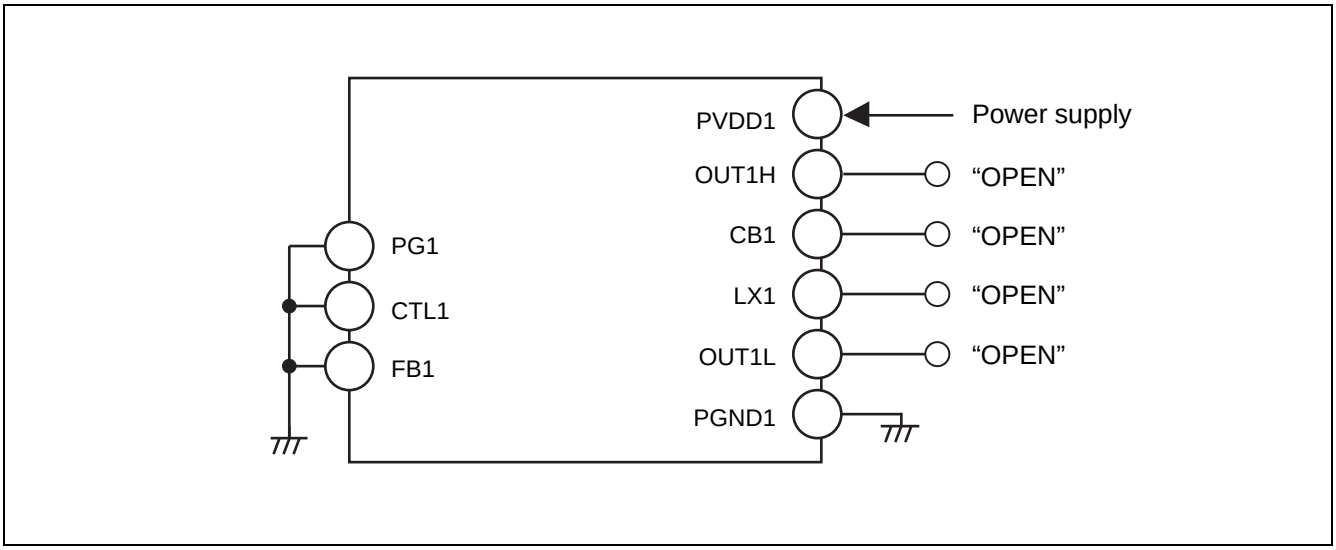


■ NOTES FOR UNCONNECTED PINS

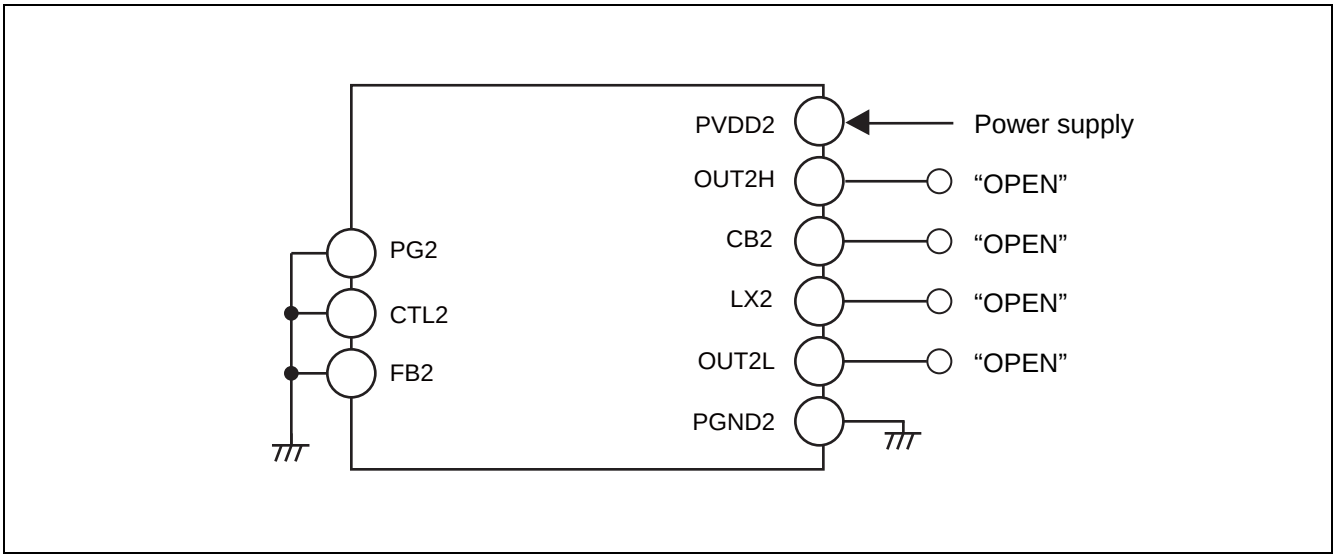
1. PIN CONNECTION WHEN NOT USING CH1 or CH2

When CH1 or CH2 are not used, connect the PVDD pins to power supply, connect the PG pins, CTL pins and FB pins to Analog ground (AGND), leave OUTH pins, OUTL pins, CB pins and LX pins open and connect the PGND pins to Power ground.

- CH1 is not used



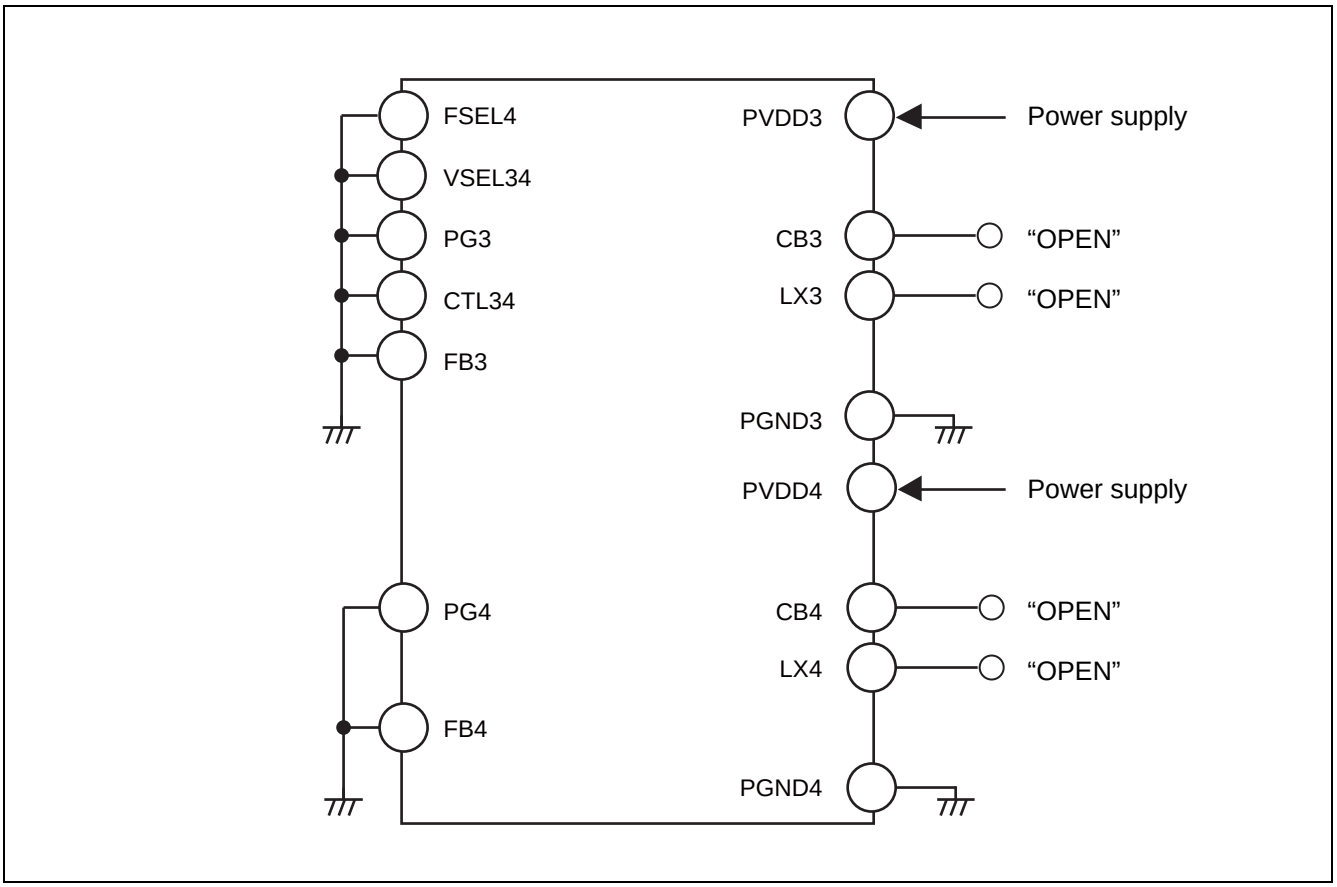
- CH2 is not used



2. PIN CONNECTION WHEN NOT USING CH3 and CH4

When CH3 and CH4 are not used, connect the PVDD pins to power supply, connect the FSEL4 pin, VSEL34 pin, PG pins, CTL34 pins and FB pins to Analog ground (AGND), leave CB pins and LX pins open and connect the PGND pins to Power ground.

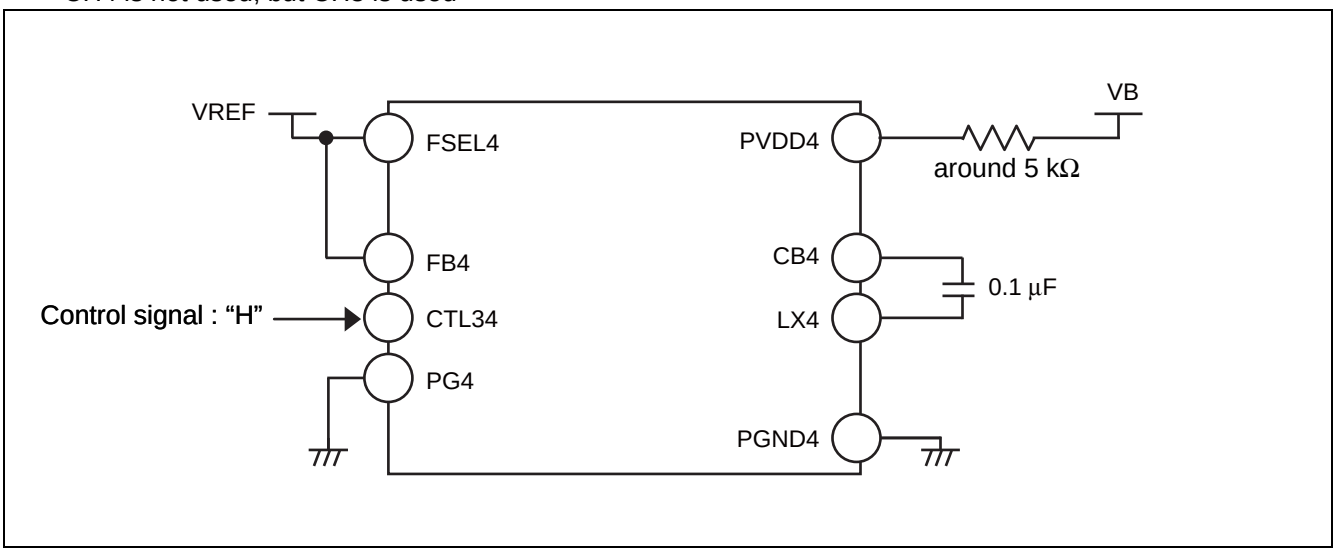
- CH3 and CH4 are not used



3. PIN CONNECTION WHEN NOT USING CH4, BUT USING CH3

When CH4 is not used but CH3 is used, connect the PVDD4 pins to VB pin through around 5 kΩ resistor, connect the PG4 pin to Analog ground (AGND), connect 0.1 µF capacitor between CB4 and LX4 pins and connect the PGND4 pin to Power ground, connect FSEL4 and FB4 pins to VREF pin.

• CH4 is not used, but CH3 is used

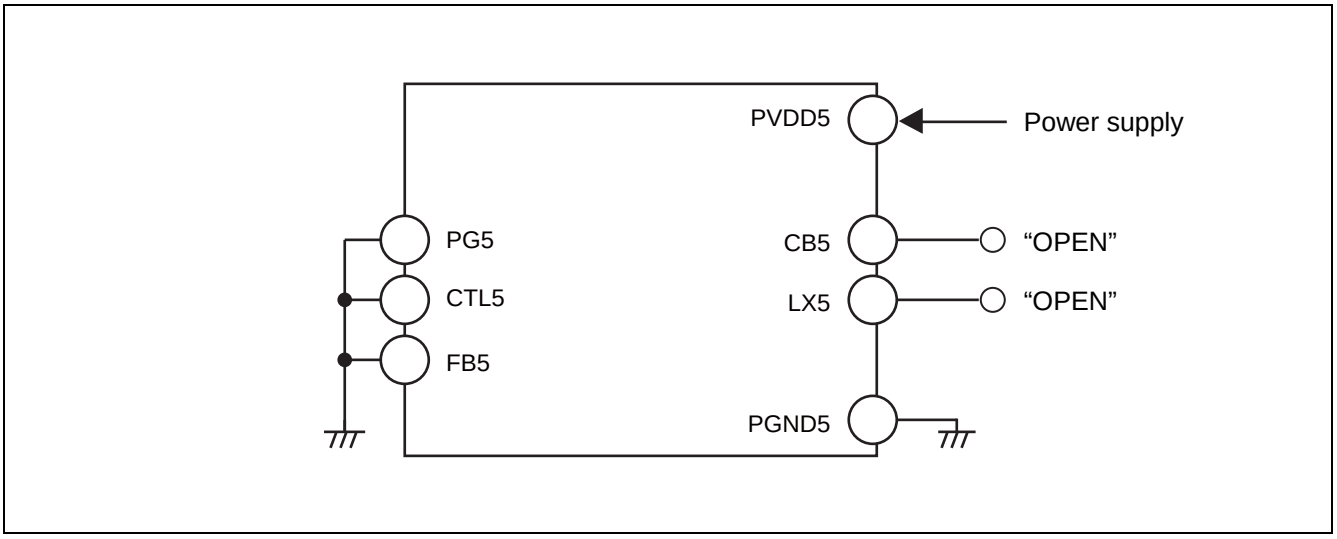


Note : Both CH3 and CH4 become active when CTL34 is on. Connect the pins like shown up above when CH4 is not used but CH3 is used. PVDD4 must not be open.

4. PIN CONNECTION WHEN NOT USING CH5

When CH5 is not used, connect the PVDD5 pins to power supply, connect the PG5, CTL5 and FB5 pins to Analog ground (AGND), leave CB5 and LX5 pins open and connect the PGND5 pin to Power ground.

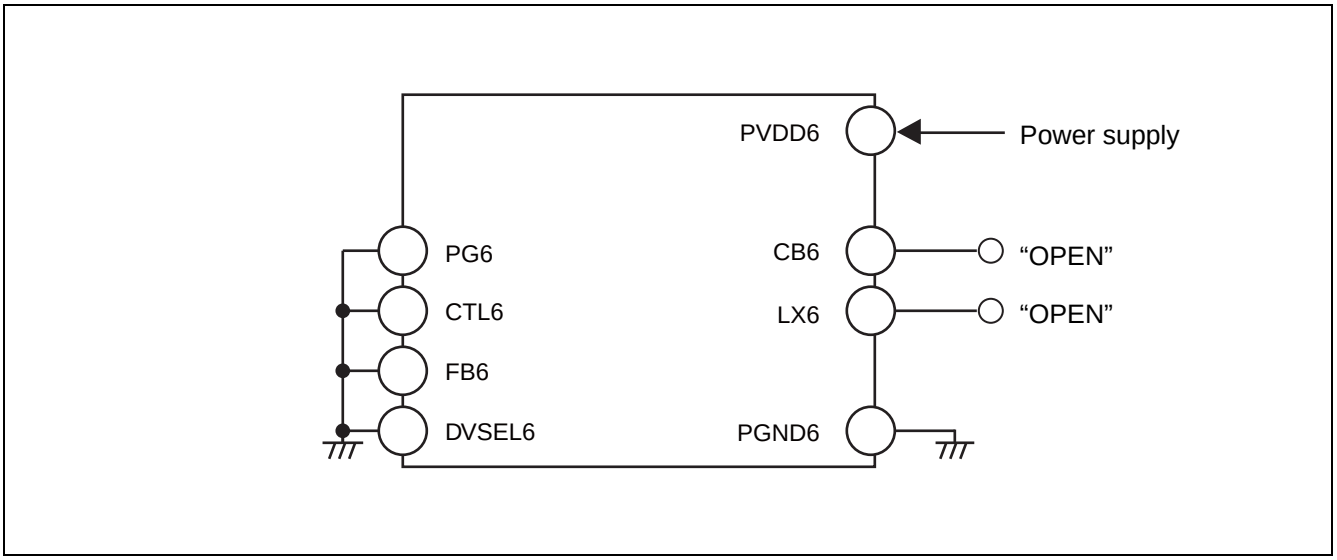
• CH5 is not used



5. PIN CONNECTION WHEN NOT USING CH6

When CH6 is not used, connect the PVDD6 pins to power supply, connect the PG6, CTL6, FB6 and DVSEL6 pins to Analog ground (AGND), leave CB6 and LX6 pins open and connect the PGND6 pin to Power ground.

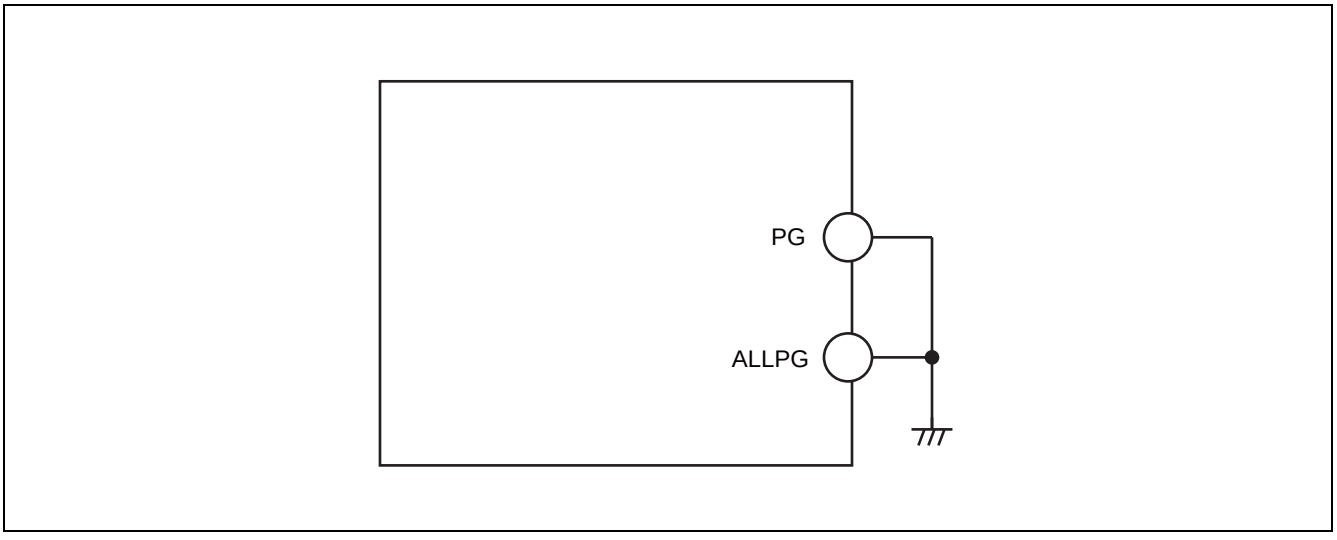
- CH6 is not used



6. PIN CONNECTION WHEN NOT USING POWERGOOD FUNCTION

When the Power good function is not used, connect the PG pins or ALLPG pin to Analog ground (AGND).

- PG or ALLPG are not used



■ APPLICATION NOTE

• Inductor Selection

See the "■RECOMMENDED OPERATING CONDITIONS" for the recommended inductance. Furthermore, to confirm whether the current flowing through the inductor is within the rated value, the maximum value of the current flowing through the inductor needs to be found. The maximum current flowing through the inductor can be found from the following formula.

$$I_{LMAX} \geq I_{OMAX} + \frac{\Delta IL}{2}$$

$$\Delta IL = \frac{V_{DD} - V_O}{L} \times \frac{V_O}{V_{DD} \times f_{OSC}}$$

I_{LMAX} : Maximum current through inductor [A]

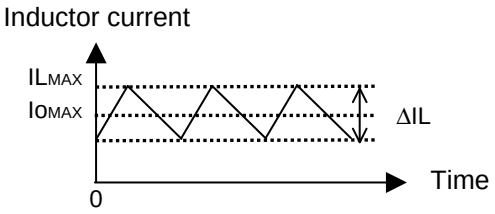
I_{OMAX} : Maximum load current [A]

ΔIL : Inductor ripple current peak-to-peak value [A]

V_{DD} : Switching power supply voltage [V]

V_O : Output setting voltage [V]

f_{OSC} : Switching frequency [Hz]



• FET Selection (CH1, CH2)

This IC operation requires the voltage which is generated between drain and source on the high-side FET. Set the on resistance of high-side FET within the below range for reference.

CH1 high-side FET on resistance : 24 mΩ to 40 mΩ
CH2 high-side FET on resistance : 12 mΩ to 20 mΩ

The current limit value for over current protection (OCP) is determined by the high-side FET on resistance in use. The current limit value is obtained by the following formula.

$$I_{O1\_OCP} = \frac{0.141}{R_{ON1}} - \frac{0.5}{L \times f_{OSC}} \times \frac{(V_{DD} - V_{O1}) \times V_{O1}}{V_{DD}}$$

$$I_{O2\_OCP} = \frac{0.133}{R_{ON2}} - \frac{0.5}{L \times f_{OSC}} \times \frac{(V_{DD} - V_{O2}) \times V_{O2}}{V_{DD}}$$

V_{DD} : Switching system power supply voltage [V]

V_O : Output setting voltage [V]

R_{ON} : High-side FET on resistance [Ω]

L : Inductor value [H]

f_{OSC} : Switching frequency [Hz]

Also, 2.5 V drive products are recommended for the high-side FET. A bootstrap diode is recommended to connect to the high-side FET for the use of 4 V drive products (see “• Bootstrap Diode Selection” for the detail).

In order to judge whether the electrical current flowing through the FET is within the rated value, the maximum value of the current flowing through the FET needs to be found. The maximum current flowing through the FET can be found from the following formula.

$$I_{DMAX} \geq I_{OMAX} + \frac{\Delta IL}{2}$$

I_{DMAX} : Maximum value of FET drain current [A]

I_{OMAX} : Maximum load current [A]

ΔIL : Inductor ripple current peak-to-peak value [A]

Furthermore, in order to judge whether the power dissipation of the FET is within the rated value, the power dissipation of the FET needs to be found. The power dissipation of the high-side FET can be found from the following formula.

$$P_{HisideFET} = P_{RON} + P_{SW}$$

$P_{HisideFET}$: High-side FET power dissipation [W]

P_{RON} : High-side FET conducting power dissipation [W]

P_{SW} : High-side FET SW power dissipation [W]

High-side FET conducting power dissipation

$$P_{RON} = (Io_{MAX})^2 \times \frac{V_O}{V_{DD}} \times R_{ON}$$

P_{RON} : High-side FET conducting power dissipation [W]

Io_{MAX} : Maximum load current [A]

V_{DD} : Switching system power supply voltage [V]

V_O : Output setting voltage [V]

R_{ON} : High-side FET on resistance [Ω]

High-side FET switching power dissipation

$$P_{SW} = \frac{V_{DD} \times f_{OSC} \times (Ibtm \times tr + Itop \times tf)}{2}$$

P_{SW} : Switching power dissipation [W]

V_{DD} : Switching system power supply voltage [V]

f_{OSC} : Switching frequency (Hz)

Ibtm : Inductor ripple current bottom value [A]

Itop : Inductor ripple current top value [A]

tr : High-side FET turn-on time [s]

tf : High-side FET turn-off time [s]

tr and tf can be found simply from the following formula.

$$tr = \frac{Qgd \times 12}{5 - Vth} \quad tf = \frac{Qgd \times 12}{Vth}$$

Qgd : Gate-Drain charge of High-side FET [C]

Vth : High-side FET threshold voltage [V]

The power dissipation of the Low-side FET can be found from the following formula.

$$P_{LosideFET} = P_{Ron} = (I_{OMAX})^2 \times \left(1 - \frac{V_O}{V_{DD}}\right) \times R_{on}$$

P_{Ron} : Low-side FET conducting power dissipation [W]

Io_{MAX} : Maximum load current [A]

V_{DD} : Switching power supply voltage [V]

V_O : Output setting voltage [V]

R_{on} : Low-side FET on resistance [Ω]

Note : The transition voltage of the voltage between the drain and source of the Low-side FET is generally small and the switching power loss is negligible. Therefore it has been omitted from this formula.

• Input Capacitor Selection

Because this IC uses the C-Mode system, it is recommended to use ceramic capacitors with a small ESR. See the "■ RECOMMENDED OPERATING CONDITIONS" for the value of the capacitance.

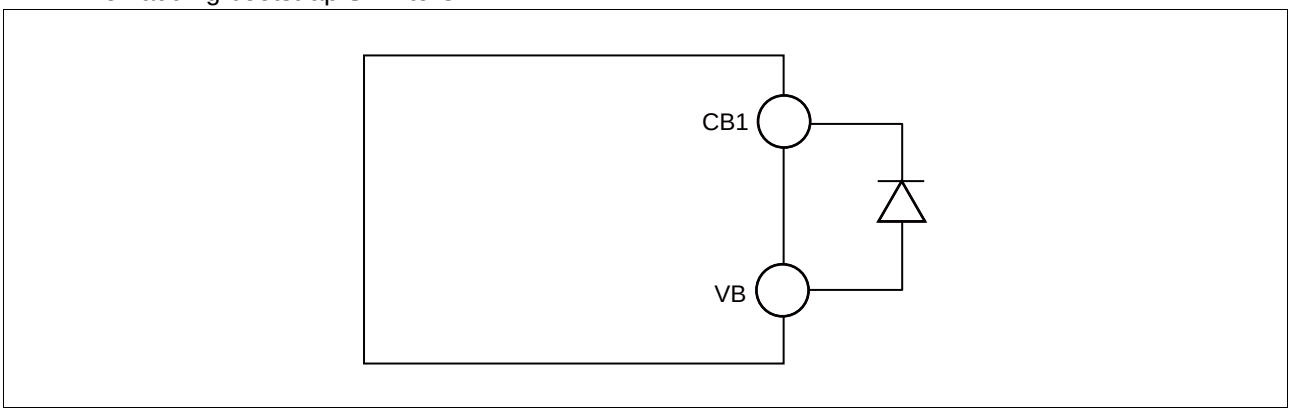
• Output Capacitor Selection

Because this IC uses the C-Mode system, it is recommended to use ceramic capacitors with a small ESR. See the "■ RECOMMENDED OPERATING CONDITIONS" for the value of the capacitance.

• Bootstrap Diode Selection

It is not necessary to connect diode to the outside device normally because this device contains a bootstrap diode. However, it is recommended to add a shotkey barrier diode (SBD) when 4 V drive products is used for CH1 and CH2 switching FET. In this case, select the smallest forward current possible and connect as the figure below.

• When adding bootstrap SBD to CH1



The current to drive on the gate of high-side FET flows to the SBD of the bootstrap diode. The average current can be found by the following formula. However, set the current which does not exceed the maximum rating.

$I_D \geq Qg \times f_{OSC}$

I_D : Forward current [A]

Qg : Total gate electric charge of high-side FET [C]

f_{OSC} : Switching frequency [Hz]

The voltage rating of bootstrap capacitor can be found by the following formula.

$V_{R\_BOOT} > V_{DD}$

V_{R_BOOT} : Bootstrap diode DC reverse voltage [V]

V_{DD} : Switching power supply voltage [V]

• Bootstrap Capacitor Selection

Although the default bootstrap capacitor (the capacitor between CB and LX) is 0.1µF, this may need to be adjusted if the FET used on CH1 and CH2 have a large Qg. The bootstrap capacitor needs to be able to charge sufficiently to drive the gate of the High-side FET. As a rough guide, select a capacitor with a minimum value of capacitance that is able to accumulate approximately 10 times the charge of the Qg of the High-side FET.

$$C_{CB} \geq 10 \times \frac{Qg}{V_{CB}}$$

C_{CB} : Bootstrap capacitance [F]

Qg : High-side SWFET gate charge [C]

V_{CB} : CB voltage (4.3 V)

• VB Capacitor Selection

Although the default VB capacitor is 1 µF, this may need to be adjusted if the FET used on CH1 and CH2 have a large Qg. The VB capacitor needs to be able to charge sufficiently to drive the gate of the High-side FET. As a rough guide, select a capacitor with a minimum value of capacitance that is able to accumulate approximately 50 times the charge of the Qg of the High-side FET.

$$C_{VB} \geq 50 \times \left(\frac{QgH_{12} + 9.3 \times 10^{-9}}{V_{CB}} + \frac{QgL_{12} + 23 \times 10^{-9}}{V_{VB}} \right)$$

C_{VB} : VB capacitance [F]

QgH_{12} : Total gate charge of High-side FET for CH1 and CH2 [C] (Total when Vgs = 4.3 V)

QgL_{12} : Total gate charge of Low-side FET for CH1 and CH2 [C] (Total when Vgs = 5 V)

V_{VB} : VB voltage (5 V)

V_{CB} : CB voltage (4.3 V)

• Power Dissipation and Thermal Design

Although these does not need to be examined in most cases because the IC is highly efficient, Dissipation and the thermal design may need to be investigate if the IC is used with high power supply voltages, high oscillator frequencies, high loads, or at high temperatures.

The internal IC power dissipation (P_{IC}) can be found from the following formula.

$$P_{IC} = V_{DD} \times (I_{DD} + Qg_{12} + 32 \times 10^{-9}) \times f_{OSC} + P_{HisideFET3\text{-}6} + P_{LosideFET3\text{-}6}$$

P_{IC} : Internal IC power dissipation [W]

V_{DD} : Power supply voltage (V_{IN}) [V]

I_{DD} : Power supply current [A] (250 μA Typ)

Qg_{12} : Total gate charge of High-side FET (V_{GS} = 4.3 V) and Low-side FET (V_{GS} = 5 V) for CH1 and CH2 [C]

f_{OSC} : Switching frequency [Hz]

$P_{HisideFET3\text{-}6}$: Total High-side SWFET power dissipation of internal High-side FET [W]

$P_{LosideFET3\text{-}6}$: Total Low-side SWFET power dissipation of internal Low-side FET [W]

Furthermore, the power dissipation of the High-side FET of each built-in channel can be found from the following formula.

$$P_{HisideFET} = P_{RON} + P_{SW}$$

$P_{HisideFET}$: High-side FET power dissipation [W]

P_{RON} : High-side FET conducting power dissipation [W]

P_{SW} : High-side FET switching power dissipation [W]

High-side FET conducting power dissipation

$$P_{RON} = (Io_{MAX})^2 \frac{V_O}{V_{DD}} \times R_{ON}$$

P_{RON} : High-side FET conducting power dissipation [W]

Io_{MAX} : Maximum load current [A]

V_{DD} : Switching power supply voltage [V]

V_O : Output setting voltage [V]

R_{ON} : On resistance of High-side FET [Ω]

High-side FET switching power dissipation

$$P_{SW} = \frac{V_{DD} \times f_{OSC} \times (Ibtm \times tr + Itop \times tf)}{2}$$

P_{SW} : SW power dissipation [W]

V_{DD} : Switching system power supply voltage [V]

f_{OSC} : Oscillation frequency (Hz)

Ibtm : Inductor ripple current bottom value [A]

Itop : Inductor ripple current top value [A]

tr : High-side FET turn-on time [s]

tf : High-side FET turn-off time [s]

tr and tf are simply given by the following values.

tr = 4 ns tf = 4 ns

The power dissipation of the Low-side FET can be found from the following formula.

$$P_{Ron} = (I_{OMAX})^2 \times \left(1 - \frac{V_O}{V_{DD}}\right) \times R_{on}$$

P_{Ron} : Low-side FET conducting power dissipation [W]

I_{OMAX} : Maximum load current [A]

V_{DD} : Switching system power supply voltage [V]

V_O : Output setting voltage [V]

R_{on} : Low-side FET on resistance [Ω]

Note : The transition voltage of the voltage between the drain and source of the Low-side FET is generally small and the switching power loss is negligible. Therefore it has been omitted from this formula.

The junction temperature (Tj) can be found from the following formula.

$Tj = Ta + \theta ja \times P_{IC}$

Tj : Junction temperature [°C] (+ 125 °C Max)

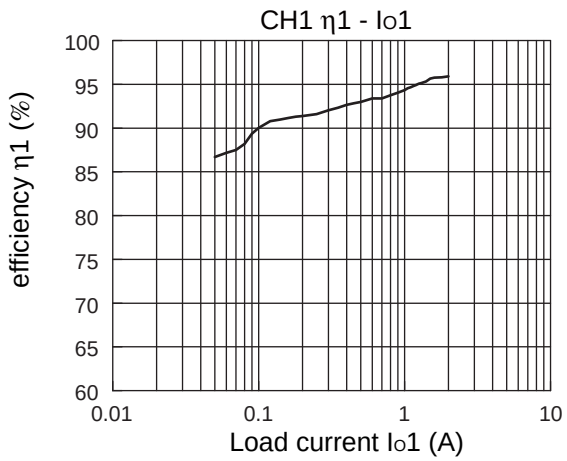
Ta : Ambient temperature [°C]

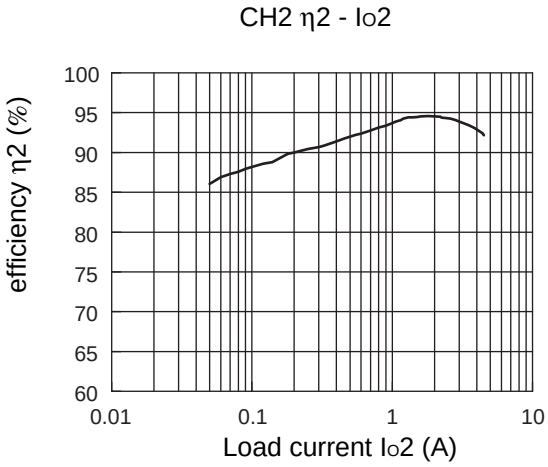
θja : PFBGA-208 package thermal resistance (34 °C/W)

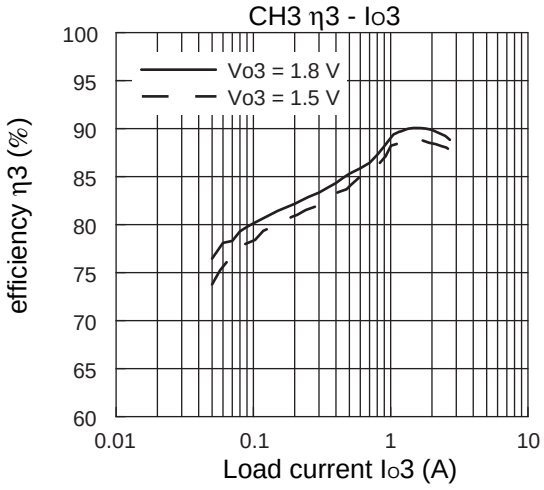
P_{IC} : IC power dissipation [W]

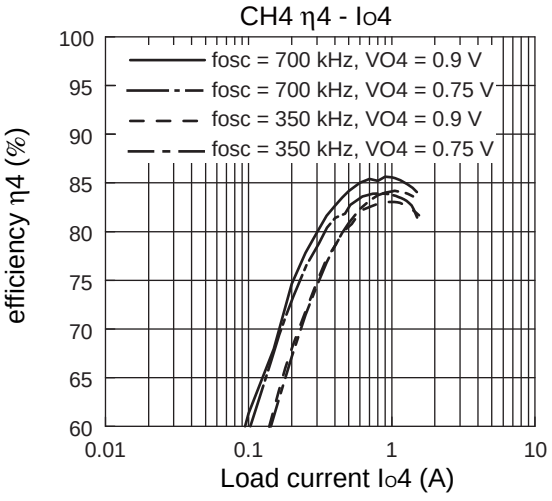
■ REFERENCE DATA

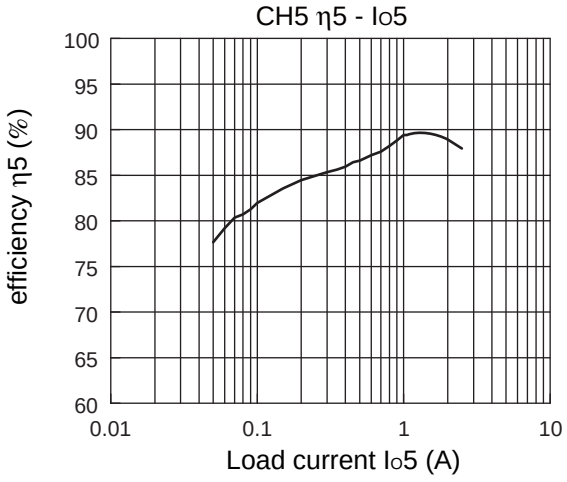
• Efficiency vs. load current

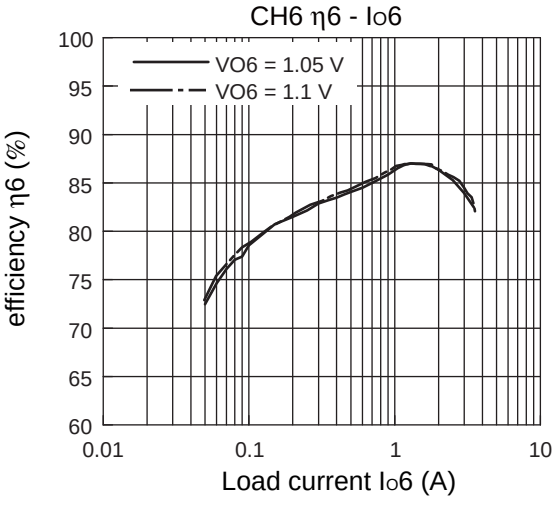




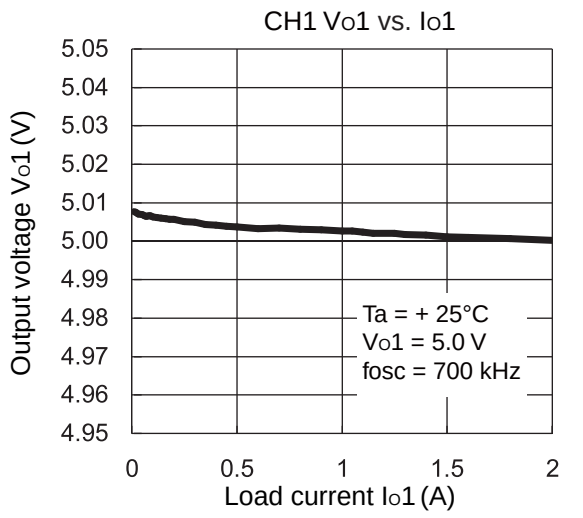


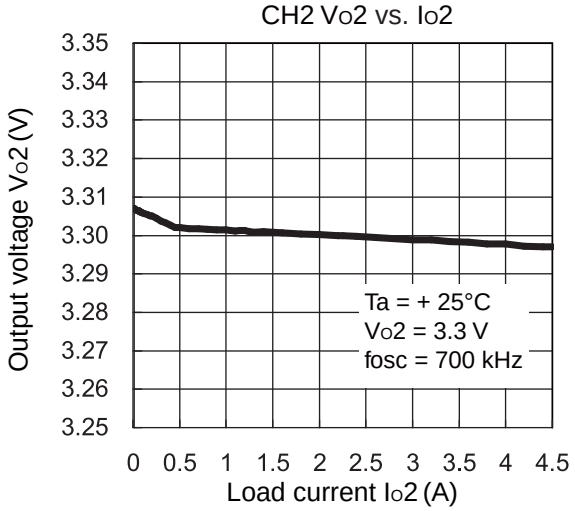


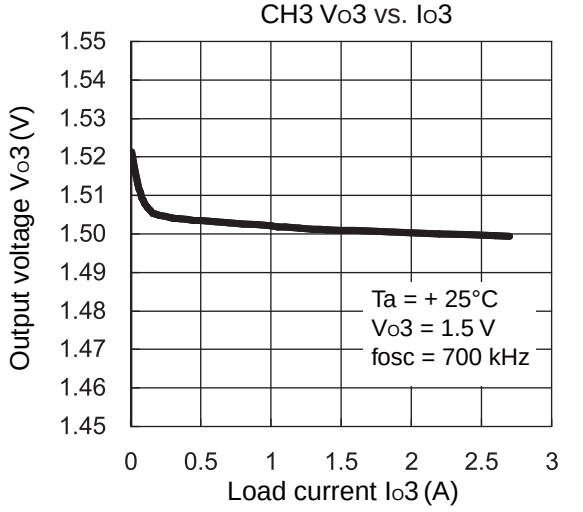


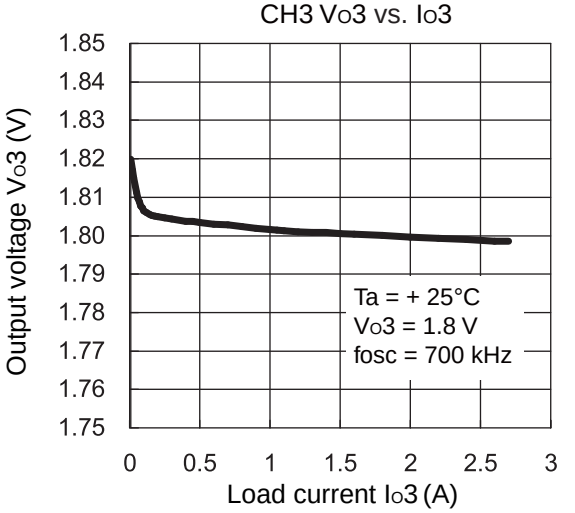


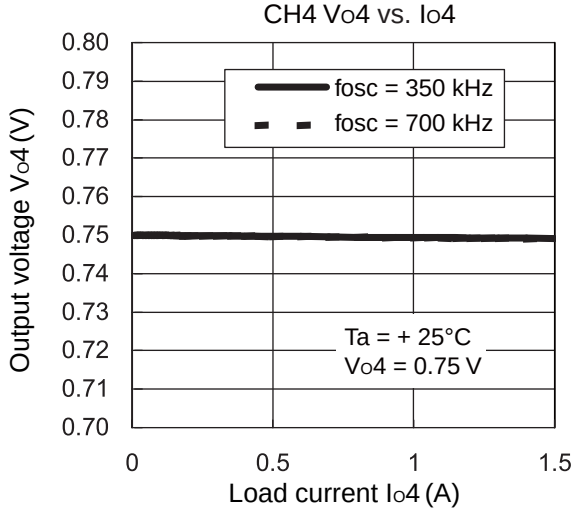
• Load regulation

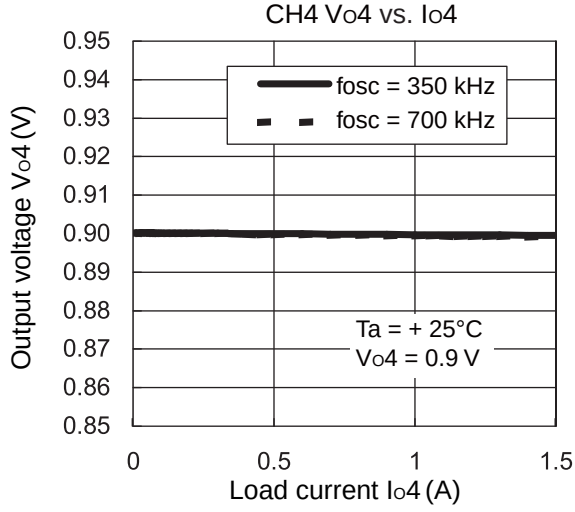












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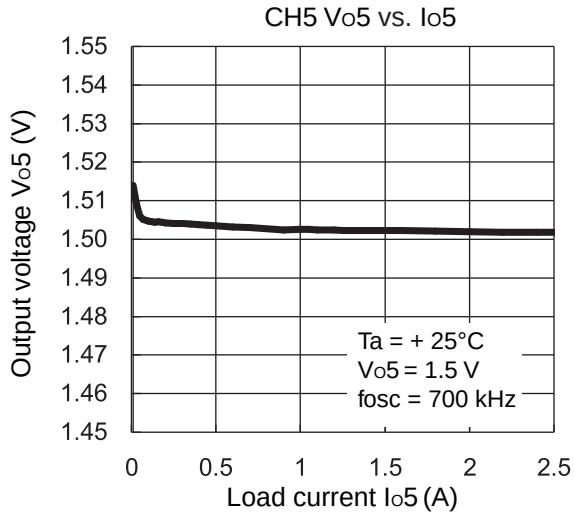
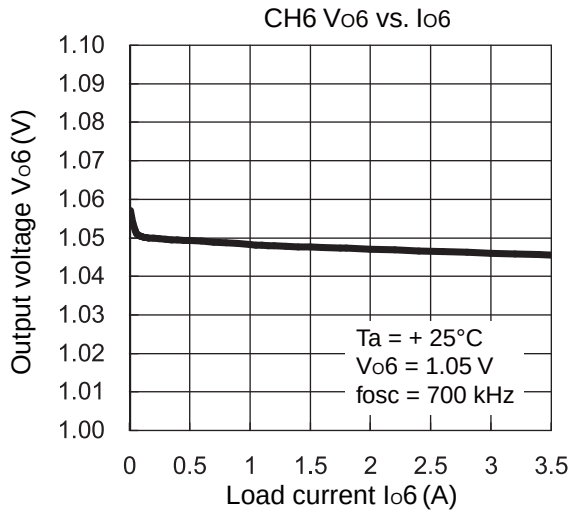
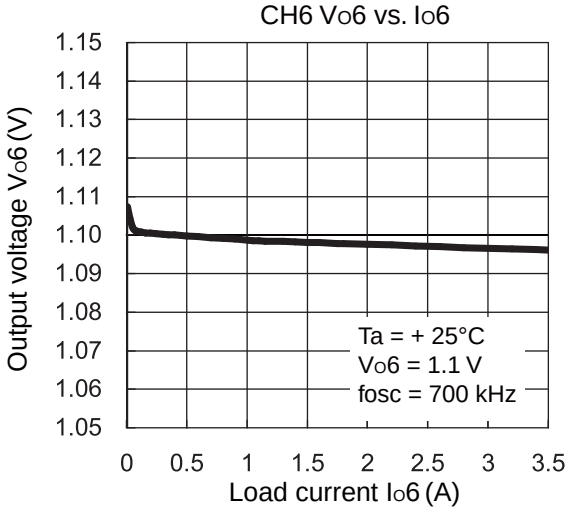
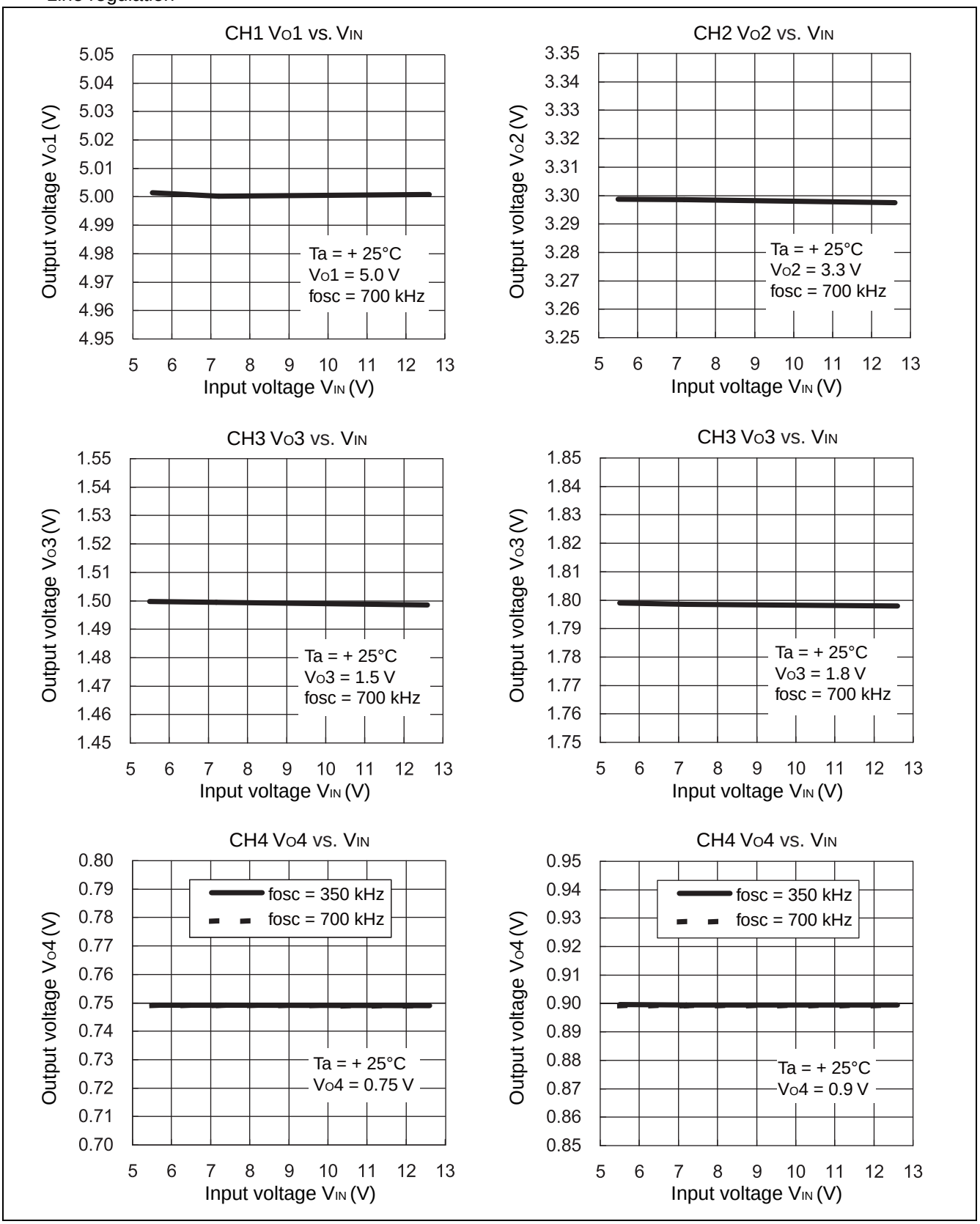

CH5 VO5 vs. IO5
Output voltage VO5 (V)
1.55
1.54
1.53
1.52
1.51
1.50
1.49
1.48
1.47
1.46
1.45
0
0.5
1
1.5
2
2.5
Load current IO5 (A)
Ta = + 25°C
VO5 = 1.5 V
fosc = 700 kHz


CH6 VO6 vs. IO6
Output voltage VO6 (V)
1.10
1.09
1.08
1.07
1.06
1.05
1.04
1.03
1.02
1.01
1.00
0
0.5
1
1.5
2
2.5
3
3.5
Load current IO6 (A)
Ta = + 25°C
VO6 = 1.05 V
fosc = 700 kHz


CH6 VO6 vs. IO6
Output voltage VO6 (V)
1.15
1.14
1.13
1.12
1.11
1.10
1.09
1.08
1.07
1.06
1.05
0
0.5
1
1.5
2
2.5
3
3.5
Load current IO6 (A)
Ta = + 25°C
VO6 = 1.1 V
fosc = 700 kHz

• Line regulation



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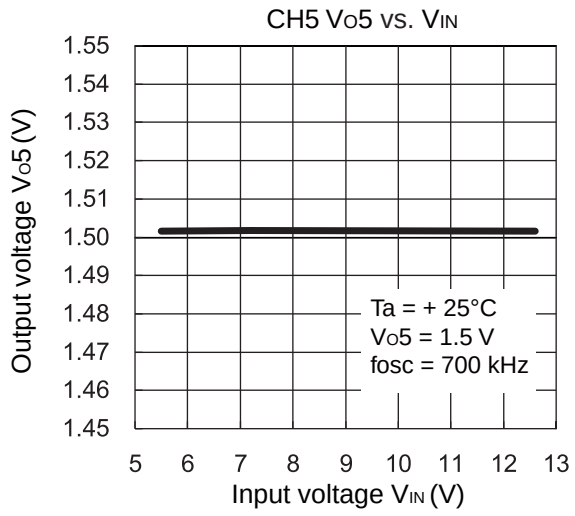
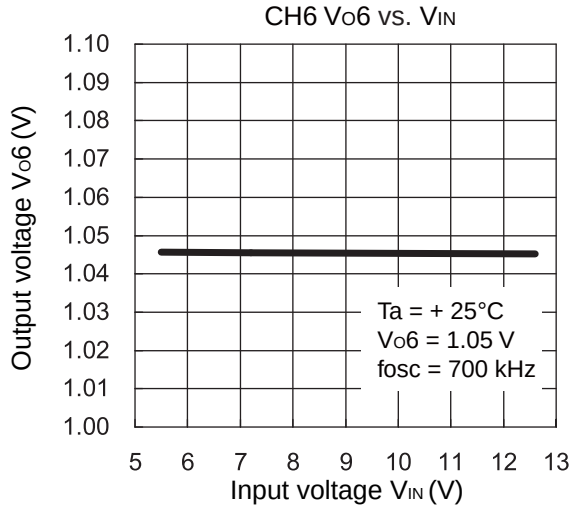
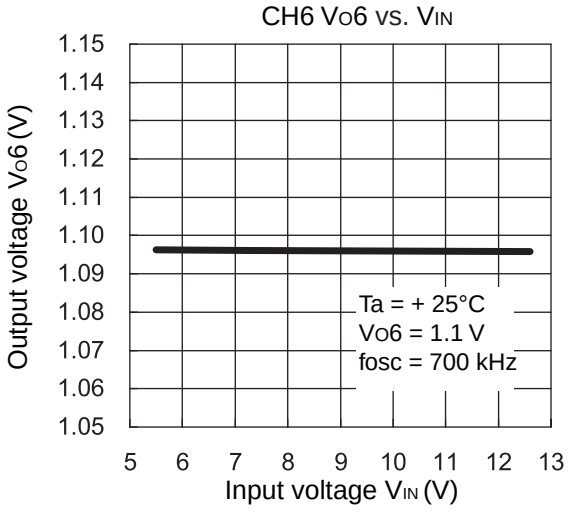
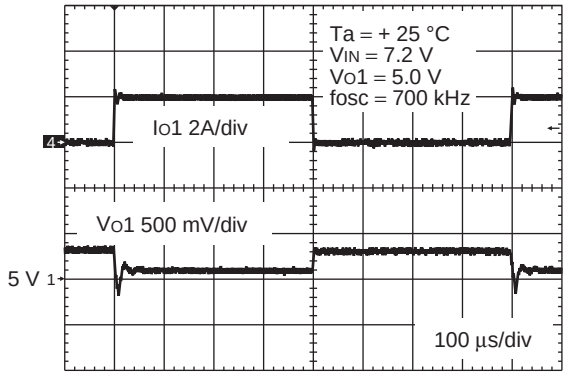

CH5 VO5 vs. VIN
Output voltage VO5 (V)
1.55
1.54
1.53
1.52
1.51
1.50
1.49
1.48
1.47
1.46
1.45
5 6 7 8 9 10 11 12 13
Input voltage VIN (V)
Ta = + 25°C
VO5 = 1.5 V
fosc = 700 kHz


CH6 VO6 vs. VIN
Output voltage VO6 (V)
1.10
1.09
1.08
1.07
1.06
1.05
1.04
1.03
1.02
1.01
1.00
5 6 7 8 9 10 11 12 13
Input voltage VIN (V)
Ta = + 25°C
VO6 = 1.05 V
fosc = 700 kHz

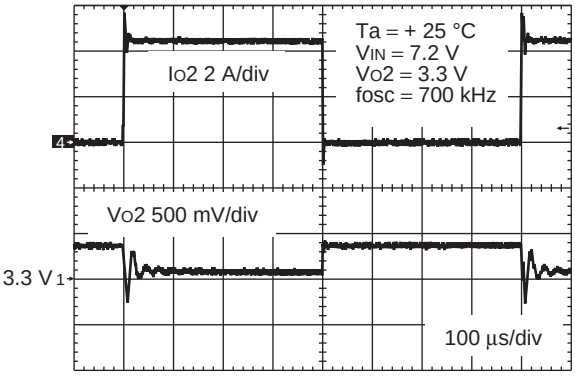

CH6 VO6 vs. VIN
Output voltage VO6 (V)
1.15
1.14
1.13
1.12
1.11
1.10
1.09
1.08
1.07
1.06
1.05
5 6 7 8 9 10 11 12 13
Input voltage VIN (V)
Ta = + 25°C
VO6 = 1.1 V
fosc = 700 kHz

- Waveforms at load step response

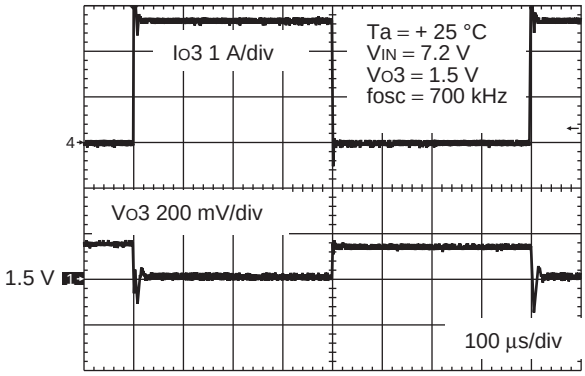
CH1 (Vo1 = 5.0 V)
Io1 = 0 A⇔ 2 A, Io1 slew rate = 2 A/µs



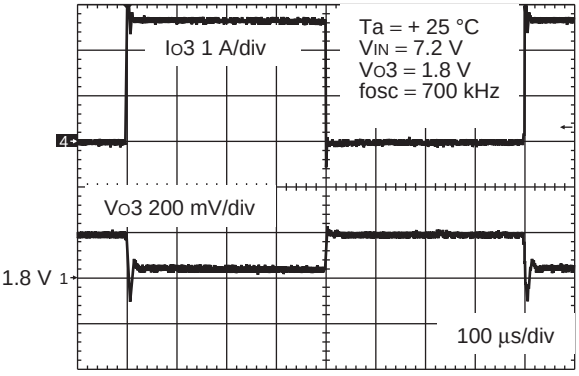
CH2 (Vo2 = 3.3 V)
Io2 = 0 A⇔4.5 A, Io2 slew rate = 4.5 A/µs



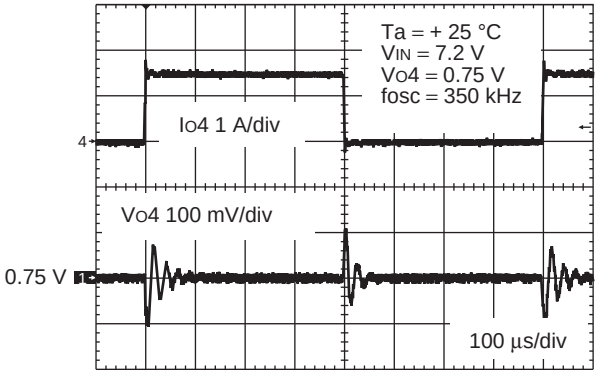
CH3 (Vo3 = 1.5 V)
Io3 = 0 A⇔2.7 A, Io3 slew rate = 2.7 A/µs



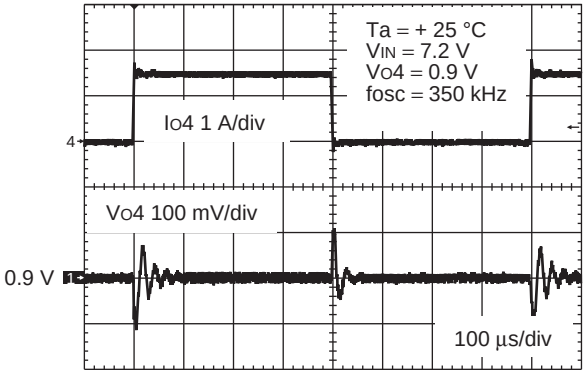
CH3 (Vo3 = 1.8 V)
Io3 = 0 A⇔ 2.7 A, Io3 slew rate = 2.7 A/µs



CH4 (fosc = 350 kHz, Vo4 = 0.75 V)
Io4 = 0 A⇔ 1.5 A, Io4 slew rate = 1.5 A/µs



CH4 (fosc = 350 kHz, Vo4 = 0.9 V)
Io4 = 0 A⇔ 1.5 A, Io4 slew rate = 1.5 A/µs



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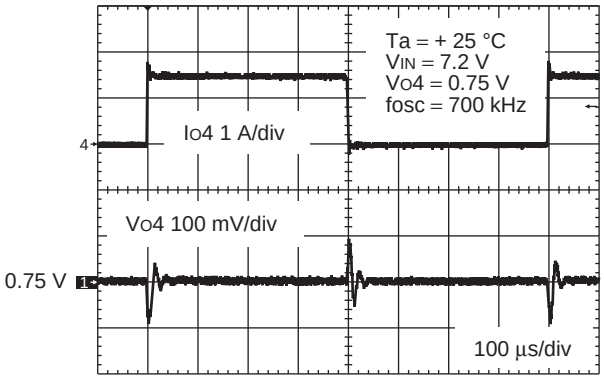
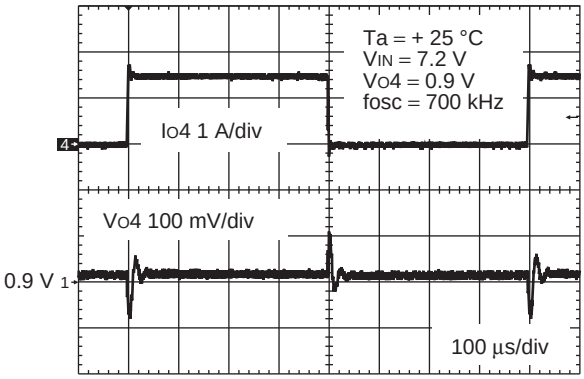
CH4 (fosc = 700 kHz, Vo4 = 0.75 V)

Io4 = 0 A⇔ 1.5 A, Io4 slew rate = 1.5 A/µs



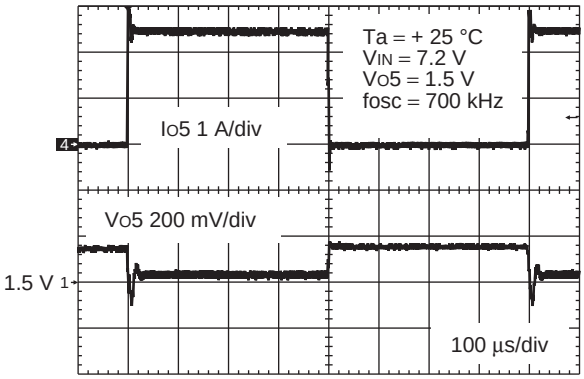
CH4 (fosc = 700 kHz, Vo4 = 0.9 V)

Io4 = 0 A⇔1.5 A, Io4 slew rate = 1.5 A/µs



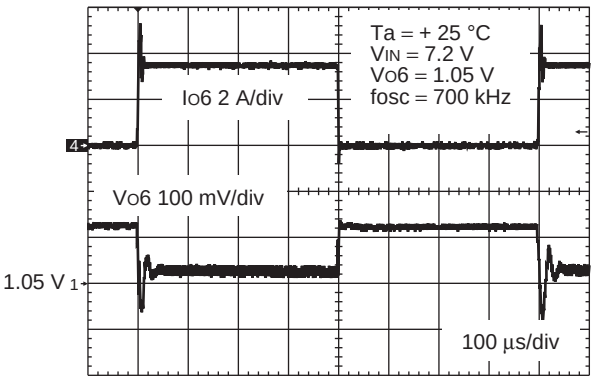
CH5 (Vo5 = 1.5 V)

Io5 = 0 A ⇔ 2.5 A, Io5 slew rate = 2.5 A/µs



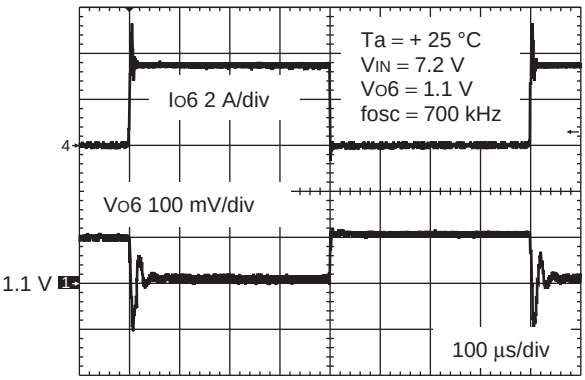
CH6 (Vo6 = 1.05 V)

Io6 = 0 A ⇔ 3.5 A, Io6 slew rate = 3.5 A/µs



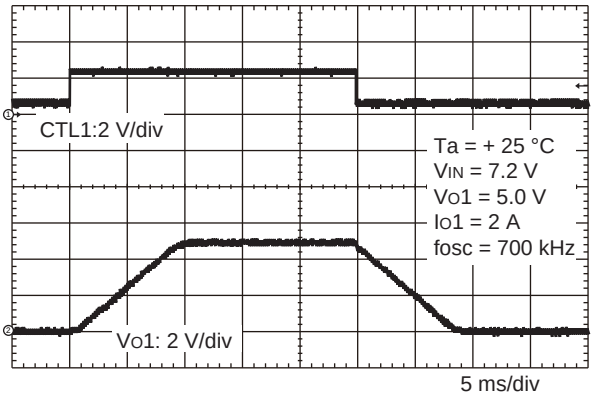
CH6 (Vo6 = 1.1 V)

Io6 = 0 A⇔3.5 A, Io6 slew rate = 3.5 A/µs

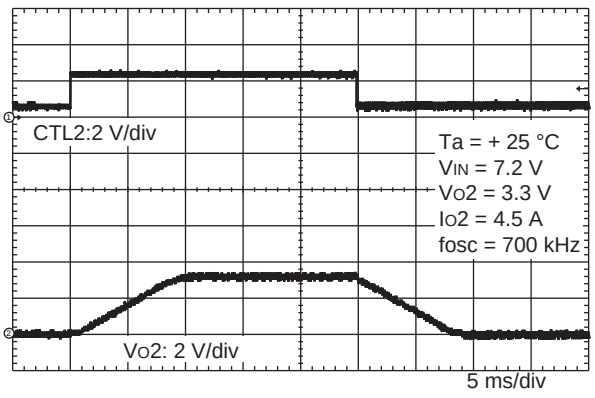


• Waveform at Soft-start and Soft-stop

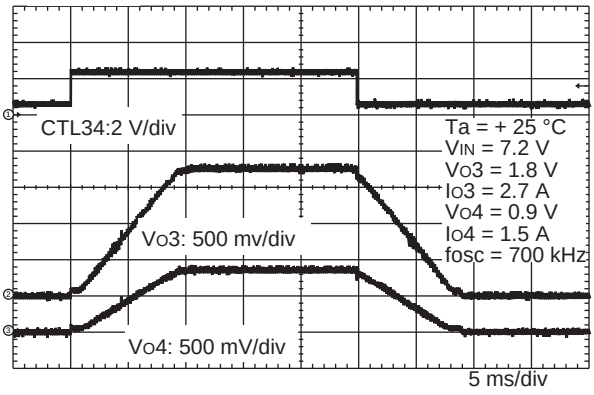
CH1



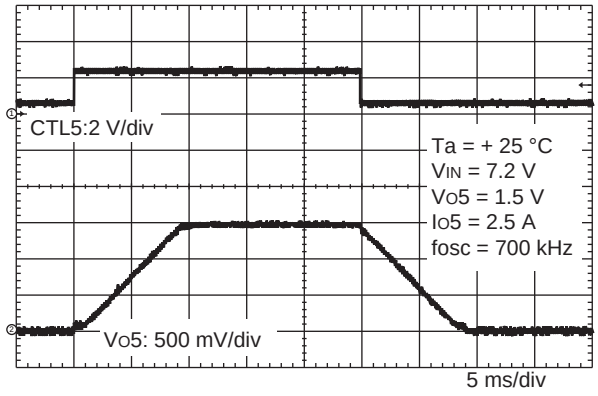
CH2



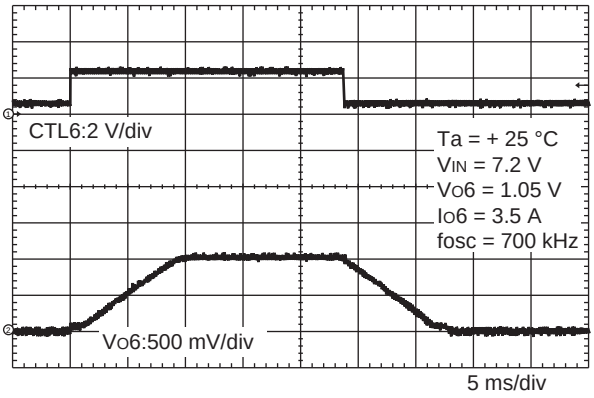
CH3, CH4



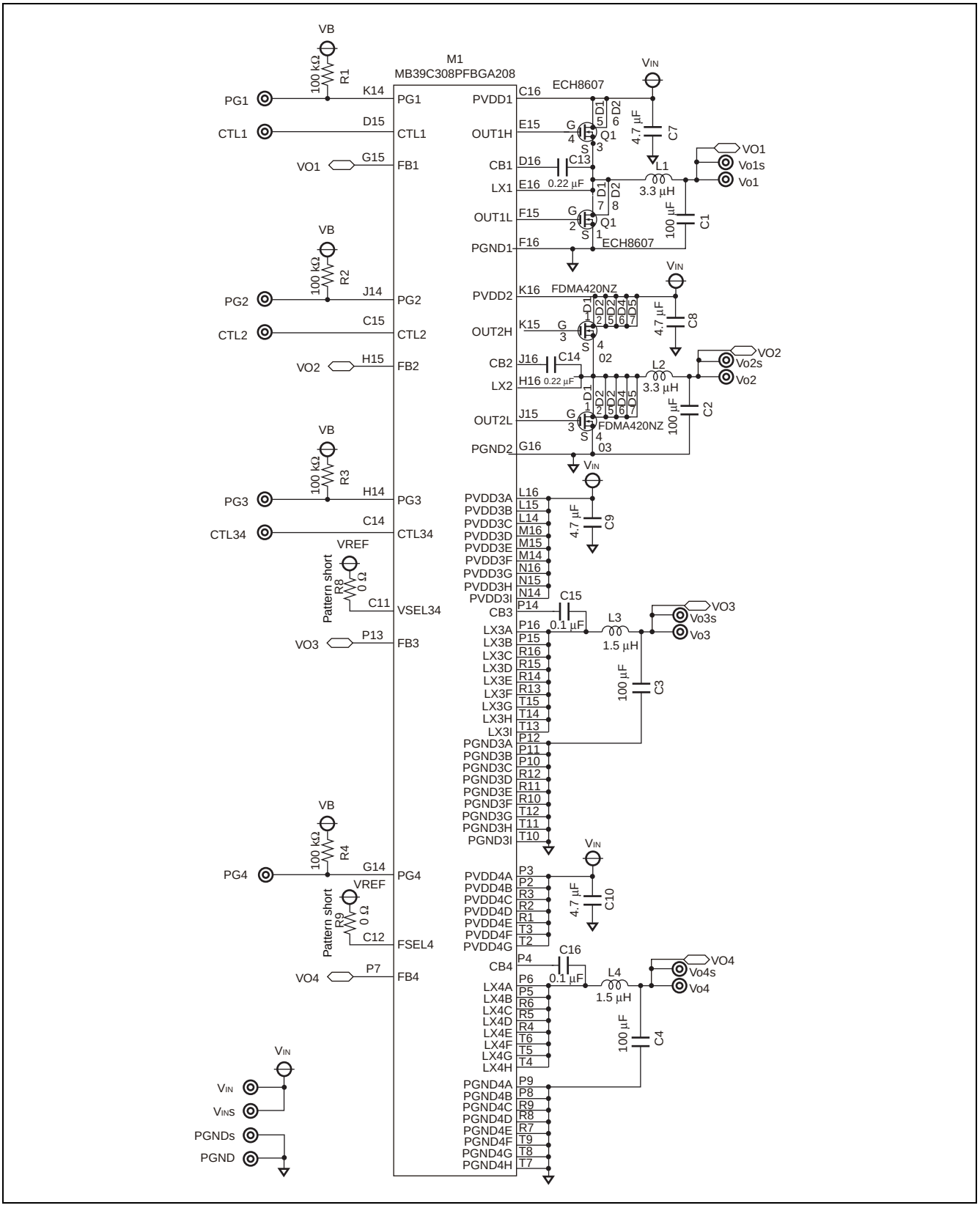
CH5



CH6



■ TYPICAL APPLICATION CIRCUIT



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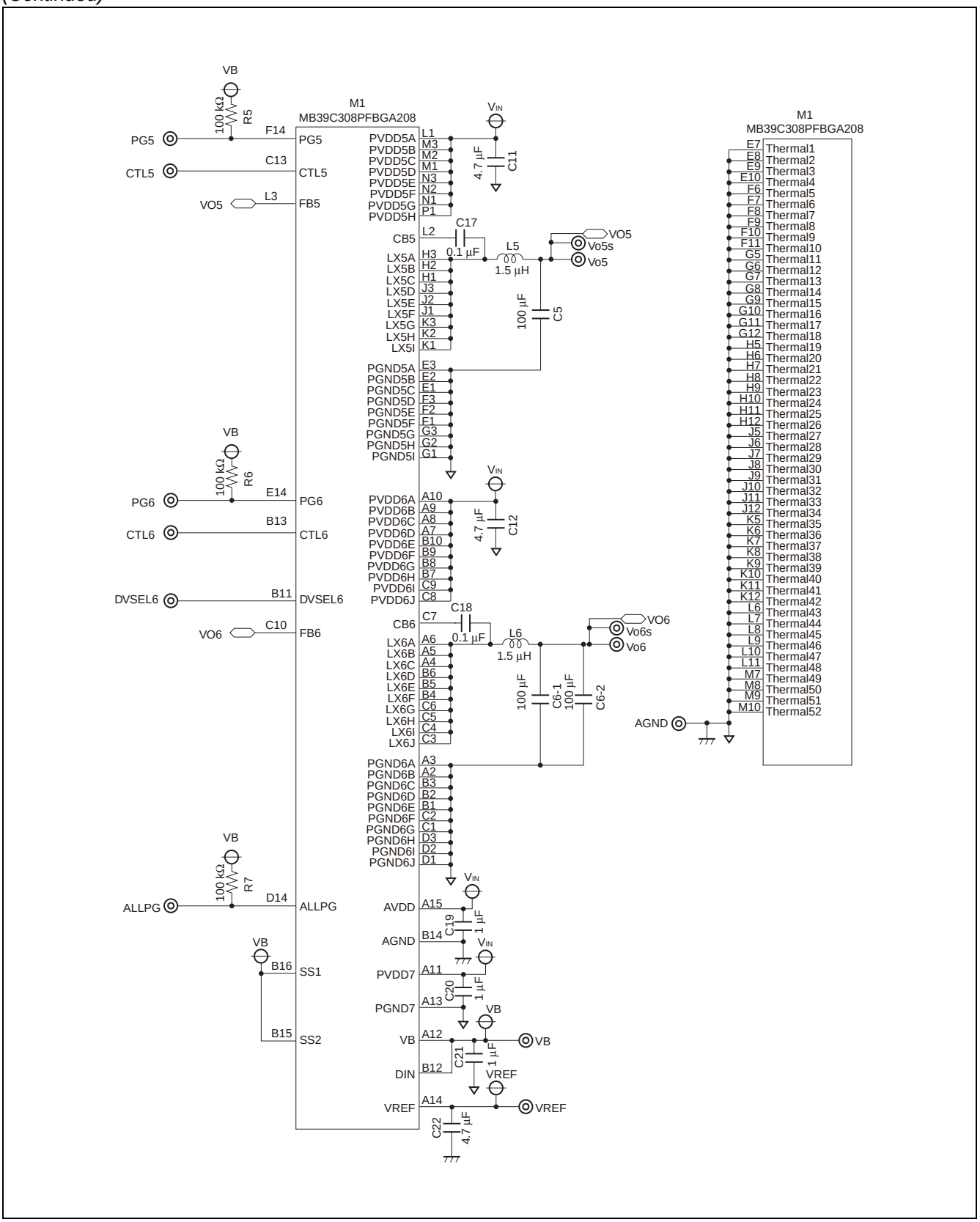
VB
100 kΩ
R5
M1
MB39C308PFBGA208
PG5
F14
PG5
CTL5
C13
CTL5
VO5
L3
FB5
VIN
4.7 µF
C11
PVDD5A
PVDD5B
PVDD5C
PVDD5D
PVDD5E
PVDD5F
PVDD5G
PVDD5H
L1
M3
M2
M1
N3
N2
N1
P1
C17
CB5
L2
0.1 µF
L5
1.5 µH
VO5
Vo5s
Vo5
LX5A
LX5B
LX5C
LX5D
LX5E
LX5F
LX5G
LX5H
LX5I
H3
H2
H1
J3
J2
J1
K3
K2
K1
100 µF
C5
PGND5A
PGND5B
PGND5C
PGND5D
PGND5E
PGND5F
PGND5G
PGND5H
PGND5I
E3
E2
E1
F3
F2
F1
G3
G2
G1
VB
100 kΩ
R6
PG6
E14
PG6
CTL6
B13
CTL6
DVSEL6
B11
DVSEL6
VO6
C10
FB6
VIN
4.7 µF
C12
PVDD6A
PVDD6B
PVDD6C
PVDD6D
PVDD6E
PVDD6F
PVDD6G
PVDD6H
PVDD6I
PVDD6J
A10
A9
A8
A7
B10
B9
B8
B7
C9
C8
C18
CB6
C7
0.1 µF
L6
1.5 µH
VO6
Vo6s
Vo6
LX6A
LX6B
LX6C
LX6D
LX6E
LX6F
LX6G
LX6H
LX6I
LX6J
A6
A5
A4
B6
B5
B4
C6
C5
C4
C3
100 µF
C6-1
100 µF
C6-2
PGND6A
PGND6B
PGND6C
PGND6D
PGND6E
PGND6F
PGND6G
PGND6H
PGND6I
PGND6J
A3
A2
B3
B2
B1
C2
C1
D3
D2
D1
VB
100 kΩ
R7
ALLPG
D14
ALLPG
VIN
AVDD
A15
C19
1 µF
AGND
B14
VIN
VB
B16
SS1
PVDD7
A11
C20
1 µF
PGND7
A13
VB
B15
SS2
VB
A12
VB
C21
1 µF
DIN
B12
VREF
VREF
A14
VREF
C22
4.7 µF
M1
MB39C308PFBGA208
E7
E8
E9
E10
F6
F7
F8
F9
F10
F11
G5
G6
G7
G8
G9
G10
G11
G12
H5
H6
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M7
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M9
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Thermal50
Thermal51
Thermal52
AGND

■ PARTS LIST

Sym-bol	Part name	Model name	Specification	Package	Vendor	Remarks
M1	IC	MB39C308	—	PFBGA-208	FML	—
Q1	N-ch Dual MOSFET	ECH8607	V_{DS} = 30 V, I_D = 5 A (Max)	ECH8	SANYO	Ch1 High & Low-side
Q2-1	N-ch MOSFET	FDMA420NZ	V_{DS} = 20 V, I_D = 5.7 A (Max)	MLP2x2-6L	FAIR-CHILD	Ch2 High-side
Q3-1	N-ch MOSFET	FDMA420NZ	V_{DS} = 20 V, I_D = 5.7 A (Max)	MLP2x2-6L	FAIR-CHILD	Ch2 Low-side
Q2-2	N-ch MOSFET	—	—	SOT-6	—	(Ch2 High-side)
Q3-2	N-ch MOSFET	—	—	TSOP-6	—	(Ch2 Low-side)
R1	Resistor	RR0816P-104-D	100 kΩ	1608	SSM	PG
R2	Resistor	RR0816P-104-D	100 kΩ	1608	SSM	PG
R3	Resistor	RR0816P-104-D	100 kΩ	1608	SSM	PG
R4	Resistor	RR0816P-104-D	100 kΩ	1608	SSM	PG
R5	Resistor	RR0816P-104-D	100 kΩ	1608	SSM	PG
R6	Resistor	RR0816P-104-D	100 kΩ	1608	SSM	PG
R7	Resistor	RR0816P-104-D	100 kΩ	1608	SSM	PG
R8	Resistor	—	Pattern short	—	—	VSEL34
R9	Resistor	—	Pattern short	—	—	FSEL4
C1	Ceramic Capacitor	C3225JB0J107M	100 µF (6.3 V)	3225	TDK	VO
C2	Ceramic Capacitor	C3225JB0J107M	100 µF (6.3 V)	3225	TDK	VO
C3	Ceramic Capacitor	GRM31CR60G107ME39L	100 µF (4 V)	3216	MURATA	VO
C4	Ceramic Capacitor	GRM31CR60G107ME39L	100 µF (4 V)	3216	MURATA	VO
C5	Ceramic Capacitor	GRM31CR60G107ME39L	100 µF (4 V)	3216	MURATA	VO
C6-1	Ceramic Capacitor	GRM31CR60G107ME39L	100 µF (4 V)	3216	MURATA	VO
C6-2	Ceramic Capacitor	GRM31CR60G107ME39L	100 µF (4 V)	3216	MURATA	VO
C7	Ceramic Capacitor	C2012JB1C475K	4.7 µF (16 V)	2012	TDK	PVDD
C8	Ceramic Capacitor	C2012JB1C475K	4.7 µF (16 V)	2012	TDK	PVDD
C9	Ceramic Capacitor	C2012JB1C475K	4.7 µF (16 V)	2012	TDK	PVDD
C10	Ceramic Capacitor	C2012JB1C475K	4.7 µF (16 V)	2012	TDK	PVDD
C11	Ceramic Capacitor	C2012JB1C475K	4.7 µF (16 V)	2012	TDK	PVDD
C12	Ceramic Capacitor	C2012JB1C475K	4.7 µF (16 V)	2012	TDK	PVDD

(Continued)

(Continued)

Symbol	Part name	Model name	Specification	Package	Vendor	Remarks
C13	Ceramic Capacitor	C1608JB1E224K	0.22 µF (25 V)	1608	TDK	CB
C14	Ceramic Capacitor	C1608JB1E224K	0.22 µF (25 V)	1608	TDK	CB
C15	Ceramic Capacitor	C1608JB1H104K	0.1 µF (50 V)	1608	TDK	CB
C16	Ceramic Capacitor	C1608JB1H104K	0.1 µF (50 V)	1608	TDK	CB
C17	Ceramic Capacitor	C1608JB1H104K	0.1 µF (50 V)	1608	TDK	CB
C18	Ceramic Capacitor	C1608JB1H104K	0.1 µF (50 V)	1608	TDK	CB
C19	Ceramic Capacitor	C1608JB1C105K	1 µF (16 V)	1608	TDK	AVDD
C20	Ceramic Capacitor	C1608JB1C105K	1 µF (16 V)	1608	TDK	PVDD7
C21	Ceramic Capacitor	C1608JB1C105K	1 µF (16 V)	1608	TDK	VB
C22	Ceramic Capacitor	C1608JB1A475K	4.7 µF (10 V)	1608	TDK	VREF
L1	Inductor	RLF7030-3R3M4R1	3.3 µH (4.1 A)	SMD	TDK	—
L2	Inductor	MPLC0730L3R3	3.3 µH (5.7 A)	SMD	NEC TOKIN	—
L3	Inductor	RLF7030-1R5N6R1	1.5 µH (6.1 A)	SMD	TDK	—
L4	Inductor	RLF7030-1R5N6R1	1.5 µH (6.1 A)	SMD	TDK	—
L5	Inductor	RLF7030-1R5N6R1	1.5 µH (6.1 A)	SMD	TDK	—
L6	Inductor	RLF7030-1R5N6R1	1.5 µH (6.1 A)	SMD	TDK	—
PIN	Wiring Terminal	WT-2-1	—	—	Mac-Eight	—

FML : FUJITSU MICROELECTRONICS LIMITED
SANYO : SANYO Electric Co.,Ltd.
FAIRCHILD : Fairchild Semiconductor Japan Ltd.
SSM : SUSUMU Co., Ltd
TDK : TDK Corporation
MURATA : Murata Manufacturing Co., Ltd.
NEC TOKIN : NEC TOKIN Corporation
Mac-Eight : Mac-Eight Co.,Ltd.

■ PRINTED CIRCUIT BOARD LAYOUT

Design of the PCB layout is important to make the suitable operation, suppressing noise or high efficiency ratio. Refer to the evaluation board layout of MB39C308EVB-01 and consider the following guideline when designing the layout of a circuit board.

1. Common items for each channel and peripheral components

• Ground and design for radiation of heat

At least, place the GND layer (PGND) in one of PCB internal layers. Place the through holes next to the GND pin of IC and each component, and connect them to the GND layer with low impedance.

Place the AGND which is separated from the GND layer with flowing large current if possible. Connect the bypass-capacitors of VREF and AVDD and the AGND pin of IC to the AGND. Connect AGND pin of IC to the GND layer by one point connection as close as possible so as not to flow a large current to the AGND. Connect GND pins of VB bypass-capacitor and the switching components to the GND layer directly.

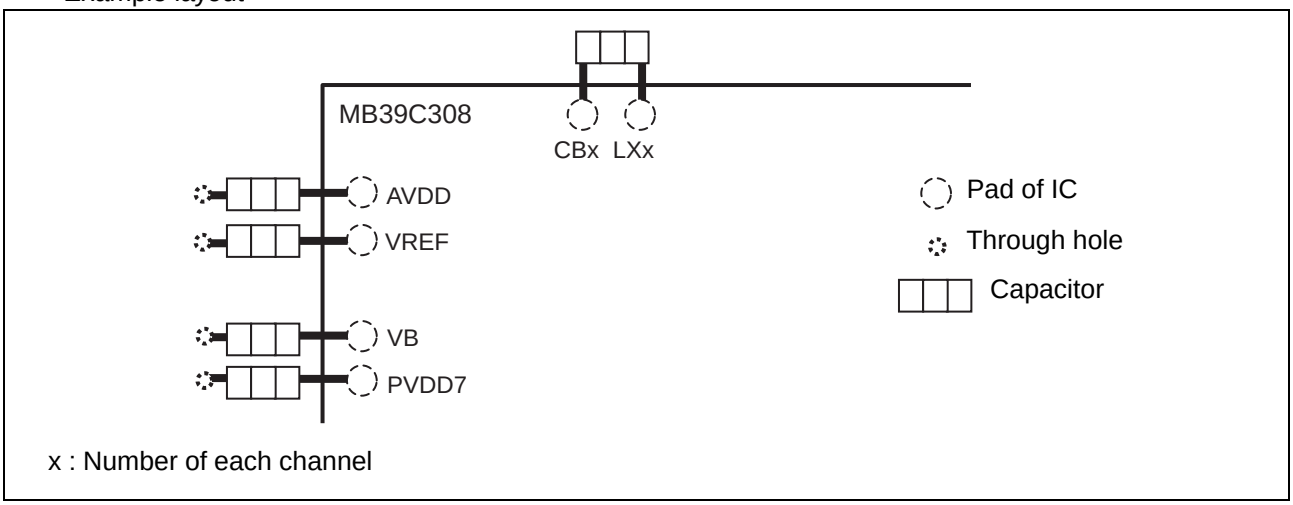
Connect each thermal pin to the GND layer via the through hole so that the heat can be dissipated efficiency. It is an ideal to place a through hole on a pad in the footprint of each thermal pin. Furthermore, it is also effective to place the GND plane on the back side of the substrate of the trace mounted on IC.

• Bypass capacitors and boot strap capacitors

Place the bypass-capacitors connected to the VREF, AVDD, VB, PVDD7 pins next to each pin of IC. Furthermore, connect the bypass-capacitors with the shortest path on surface layer to each pin. Place GND pins of bypass-capacitors connected to VB and PVDD7 pins to the PGND7 pin with the shortest path.

Place the bootstrap capacitors for each channel next to CBx and LXx pins.

• Example layout

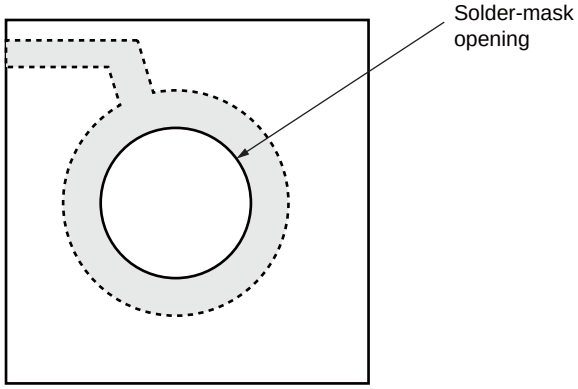


• Feedback line

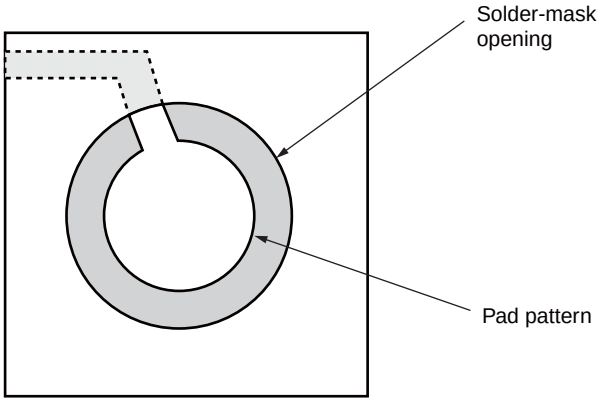
Place the feed back lines to FB pins for each channel away from switching components and lines, because the feed back line is sensitive to noise.

• Printed circuit board design rule for PFBGA

■ SMD



■ NSMD



	SMD (solder-mask defined)		NSMD (non-solder mask defined)	
	Pad pattern	**Solder-mask opening**	**Pad pattern**	**Solder-mask opening**
0.5 mm pitch	ϕ0.325 to ϕ0.35	ϕ0.225 to ϕ0.25	ϕ0.225 to ϕ0.25	ϕ0.325 to ϕ0.35

2. External switching FET channel (CH1, CH2)

For the loop consisting of the input capacitor (C_{IN}), high-side FET and low-side FET of each channel, take the most care of making the current loop as tight as possible.

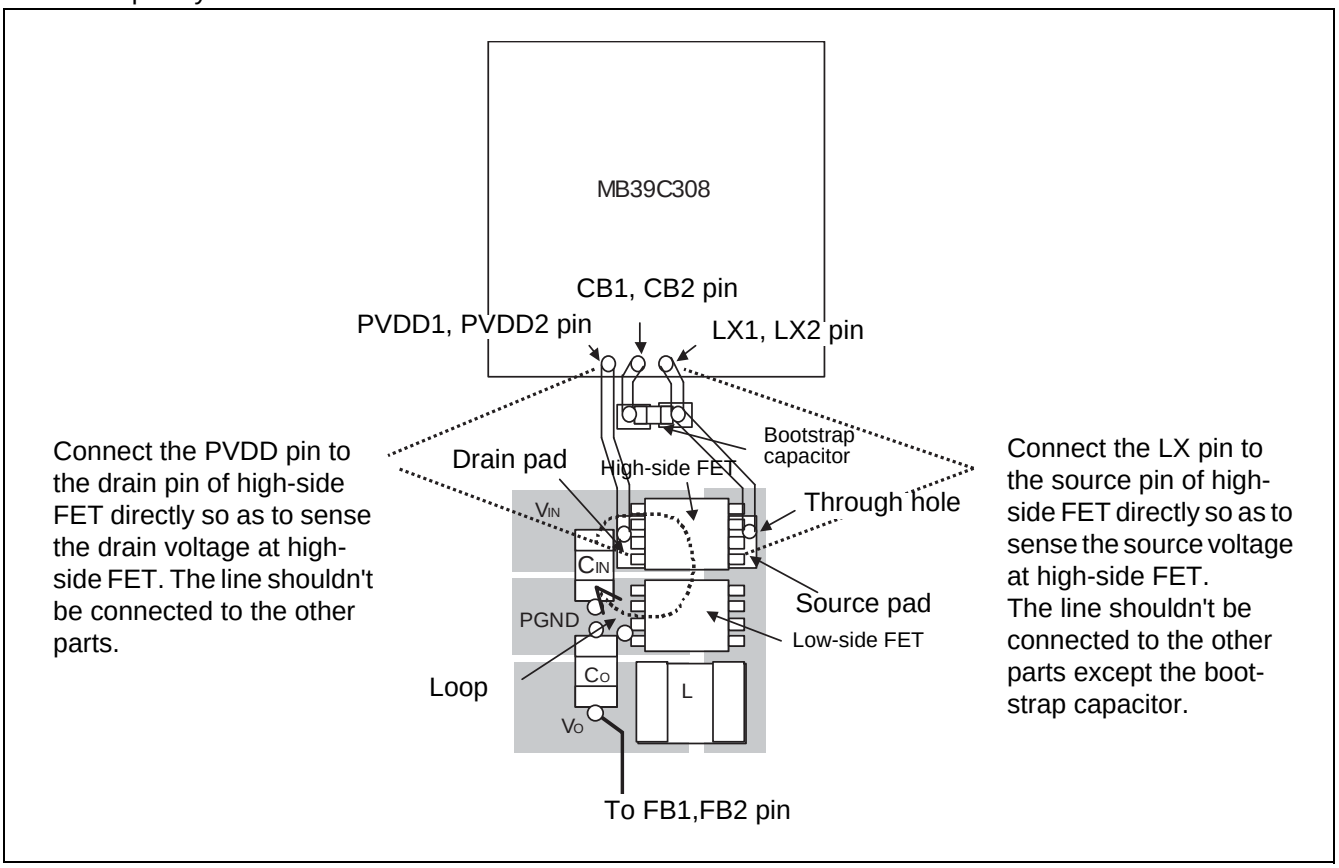
The input capacitor (C_{IN}), high-side FET and low-side FET, inductor (L) and output capacitor (C_O) should be connected to the surface layer as much as possible using short and thick connections. In addition, avoid making connections to theses components via the through hole.

Large transient current flows through the connections between the FET gate and OUT1H,OUT1L,OUT2H and OUT2L pins. Make this lines as short and thick as possible (ex. 0.5 mm width).

PVDD1, PVDD2, LX1, LX2 pins sense the voltage between drain and source at high-side FET. Connect the PVDD1 or PVDD2 pin to the drain pin of high-side FET directly. Avoid connecting to the other part on the line. Connect the LX1 or LX2 pin to the source pin of high-side FET directly. Connect the bootstrap capacitor as in the following graph and avoid connecting to the other part on the line. Furthermore, large transient current also flows through the connection to the LX pin. Make the line as short and thick as possible (exp: PVDD1, PVDD2, LX1, LX2 lines are 0.5 mm width).

When not connecting the PVDD and the LX pins to the drain or the source pin of the high-side FET as the layout below, an error may occur in PWM/PFM switch current value and the OCP setting value because of the error occurred in the current sense value.

- Example layout

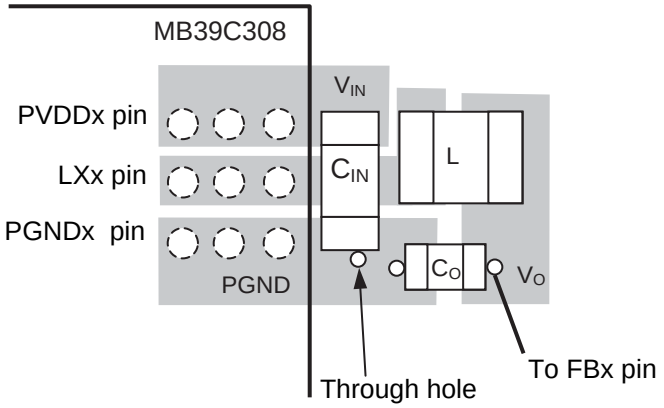


3. Internal switching FET channel (CH3 to CH6)

Place the input capacitor (C_{IN}) for each channel next to PVDDx and PGNDx pins as in the following graph.

The PVDDx, LXx, PGNDx pins, input capacitor (C_{IN}), inductor (L) and output capacitor (C_O) should be connected to the surface layer as much as possible using short and thick connections. Avoid connecting these components via the through hole.

- Example layout



x : Number of channel

■ USAGE PRECAUTION

1. Do not configure the IC over the maximum ratings

If the IC is used over the maximum ratings, the LSI may be permanently damaged.
It is preferable for the device to normally operate within the recommended usage conditions. Usage outside of these conditions can have a bad effect on the reliability of the LSI.

2. Use the devices within recommended operating conditions

The recommended operating conditions are under which the LSI is guaranteed to operate.
The electrical ratings are guaranteed when the device is used within the recommended operating conditions and under the conditions stated for each item.

3. Printed circuit board ground lines should be set up with consideration for common impedance

4. Take appropriate measures against static electricity

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

5. Do not apply negative voltages

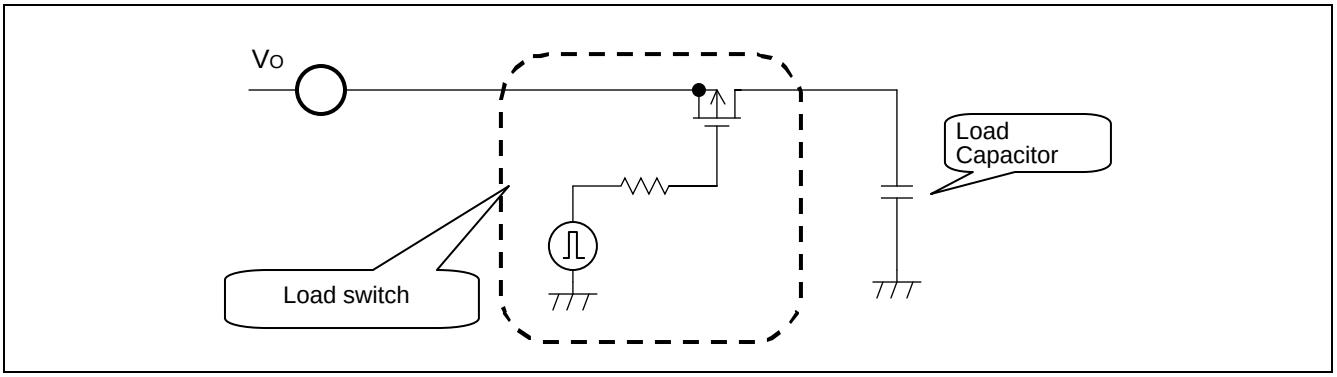
The use of negative voltages below –0.3 V may create parasitic transistors on LSI lines, which can cause malfunctions.

6. Warnings when connecting the load

During DC/DC operation, if the output is connected by hard switching to a capacitance that greatly exceeds the DC/DC output capacitance, the output voltage may oscillate and the protection function may be detected due to the instant voltage drop. Take note of the following points.

- Connecting to the load capacitor

A P-ch FET is normally used as a load switch, and a gate resistor is inserted as shown below for the switch to turn on gradually and to prevent rush current.



7. Partial short circuits

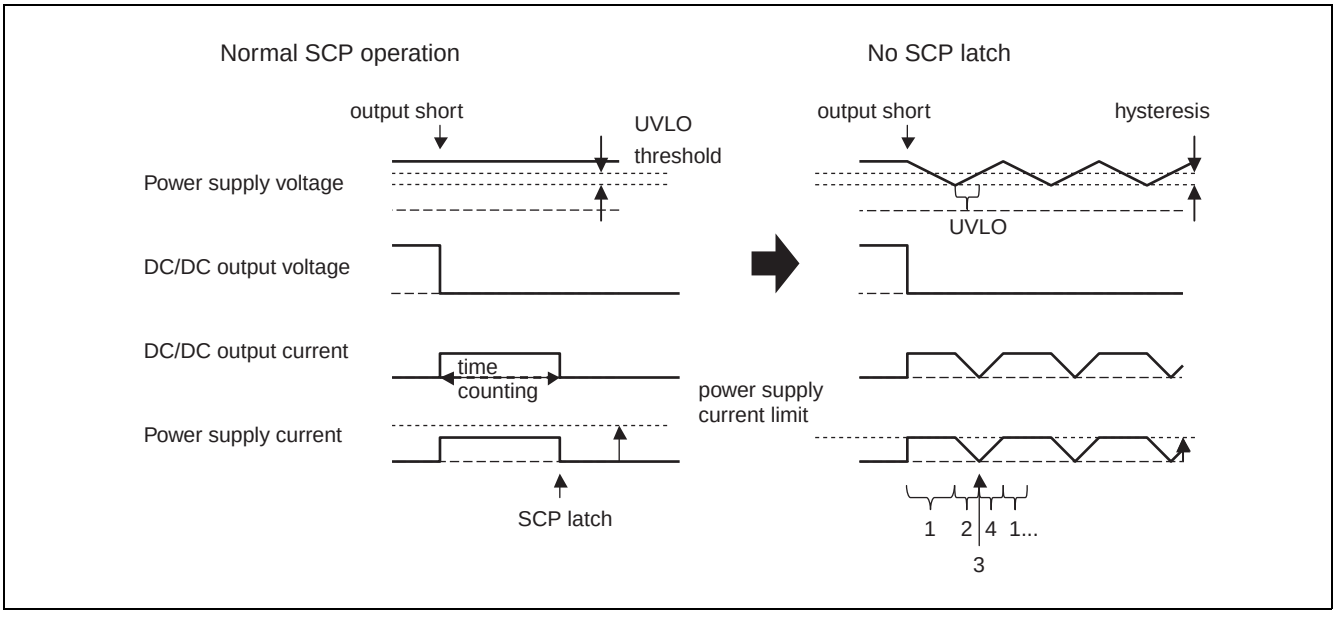
Normally, in the event of a short circuit, such as the DC/DC output connecting to ground or low potential point, output is stopped by the short circuit protection (SCP) function. Take care in the event of a partial short circuit, because the output is not stopped by the short circuit protection (SCP) function. It is recommended that a fuse be inserted into the input. If the short circuit conditions partially occur in several channels which contain the FET, there is a possibility of smoke or fire.
[Partial short circuit : Refers to a short circuit condition where overcurrent flows but is not strong enough to decrease the output voltage.]

8. Affects of insufficient power supply capacity on the SCP latch function

If the large current exceeding the current limit of input power supply flows through this device such as the case of output short, power supply voltage may drop. On such occasion, if the power supply voltage drops below 5 V (Typ) before it detects SCP, DC/DC output is shutdown by the UVLO (Under Voltage Lock Out) function. After the DC/DC output is shutdown, the input power supply recovers and SCP timer is reset, then the DC/DC converter starts operating again. As the results, the DC/DC output does not stop at SCP latch function, and the following four processes are repeated in the following order. In addition, it should be noted that under the above conditions, some components of the DC/DC converter may be destroyed.

1. Power supply voltage drops as power supply current reaches its limit.
2. DC/DC output is shutdown by UVLO.
3. UVLO is released.
4. Output current and power supply current increase.

It is recommended that a fuse be inserted into the power line. If output wires are short-circuited in the multiple channels which contain the FET, there is a possibility of smoke or fire.



■ ORDERING INFORMATION

Part number	Package	Remarks
MB39C308BGF	208-ball plastic PFBGA (BGA-208P-M02)	

■ EV BOARD ORDERING INFORMATION

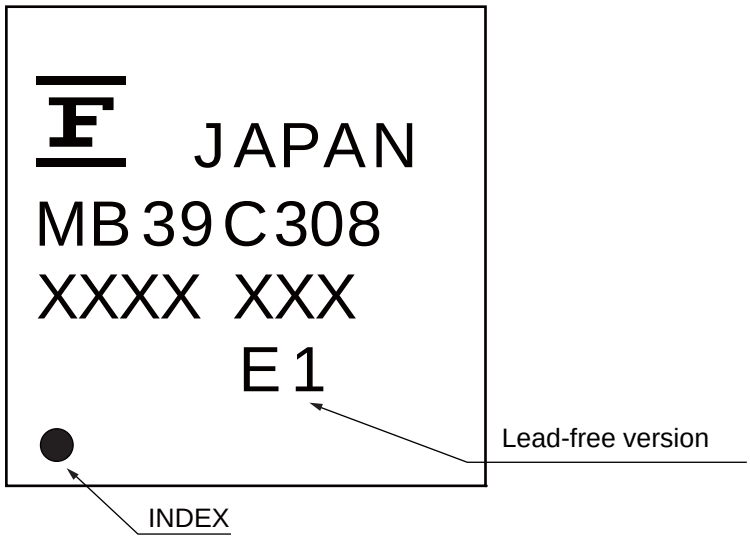
EV board part No.	EV board version No.	Remarks
MB39C308EVB-11	Board rev.1.0	PFBGA-208

■ RoHS COMPLIANCE INFORMATION OF LEAD (Pb) FREE VERSION

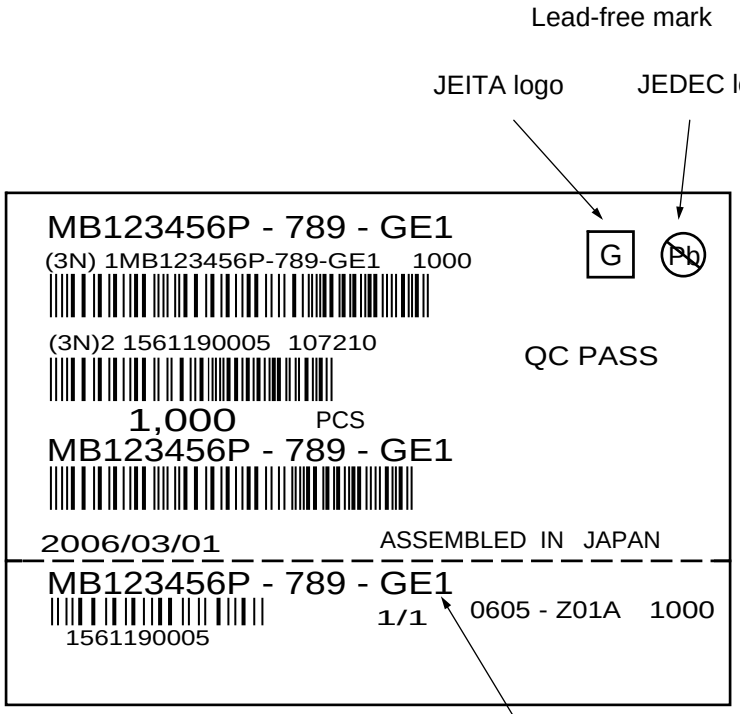
The LSI products of Fujitsu Microelectronics with “E1” are compliant with RoHS Directive , and has observed the standard of lead, cadmium, mercury, hexavalent chromium, polybrominated biphenyls (PBB) , and polybrominated diphenyl ethers (PBDE) .

A product whose part number has trailing characters “E1” is RoHS compliant.

■ MARKING FORMAT (LEAD FREE VERSION)



■ LABELING SAMPLE (LEAD FREE VERSION)



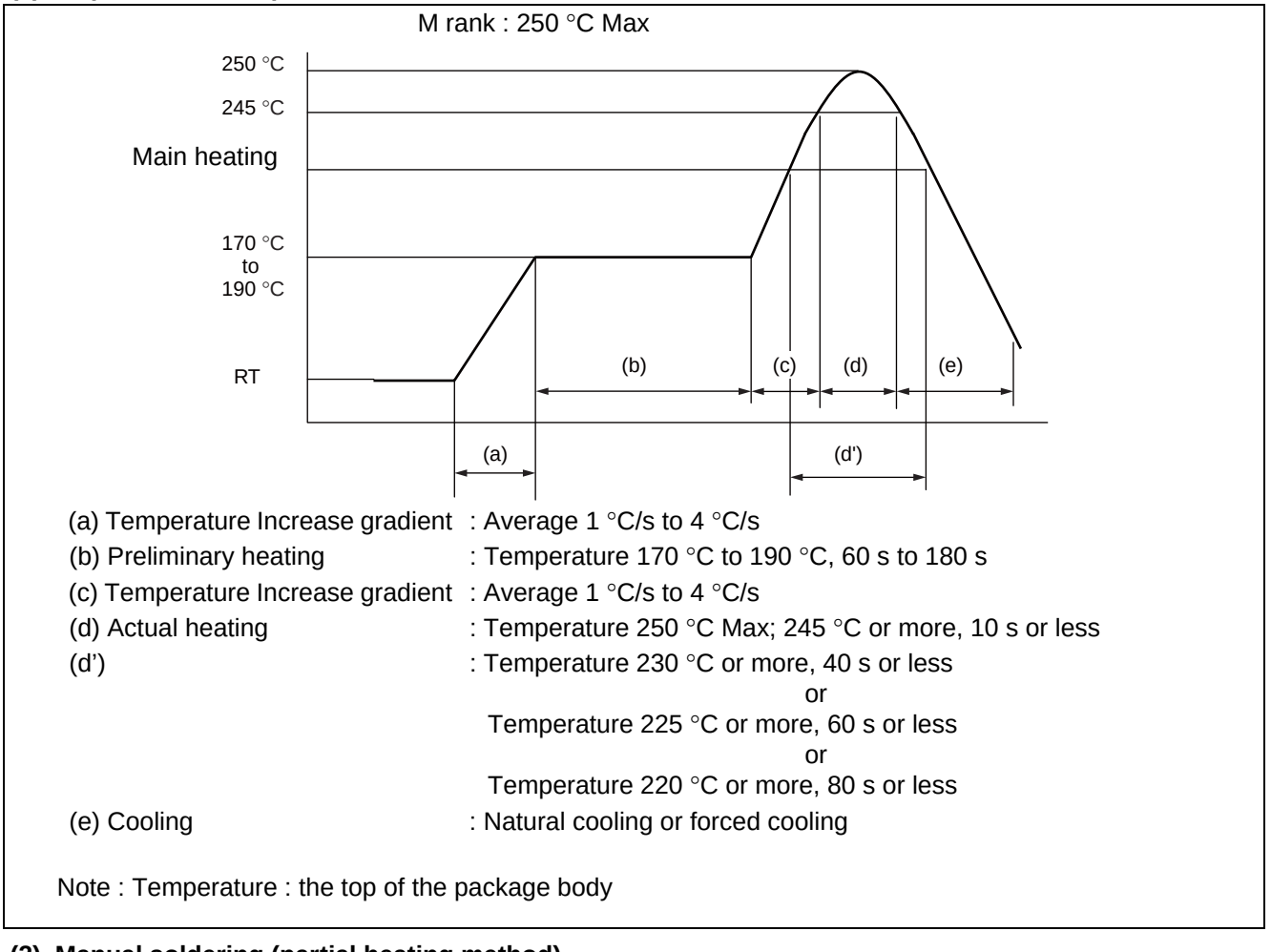
■ MB39C308BGF
RECOMMENDED CONDITIONS OF MOISTURE SENSITIVITY LEVEL

[Fujitsu Microelectronics Recommended Mounting Conditions]

Item	Condition	
Mounting Method	IR (infrared reflow) , Manual soldering (partial heating method)	
Mounting times	2 times	
Storage period	Before opening	Please use it within two years after Manufacture.
	From opening to the 2nd reflow	Less than 6 days
	When the storage period after opening was exceeded	Please processes within 6 days after baking (125 °C, 24H)
Storage conditions	5 °C to 30 °C, 70%RH or less (the lowest possible humidity)	

[Temperature Profile for FJ Standard IR Reflow]

(1) IR (infrared reflow)



(a) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(b) Preliminary heating : Temperature 170 °C to 190 °C, 60 s to 180 s
(c) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(d) Actual heating : Temperature 250 °C Max; 245 °C or more, 10 s or less
(d') : Temperature 230 °C or more, 40 s or less
or
Temperature 225 °C or more, 60 s or less
or
Temperature 220 °C or more, 80 s or less
(e) Cooling : Natural cooling or forced cooling

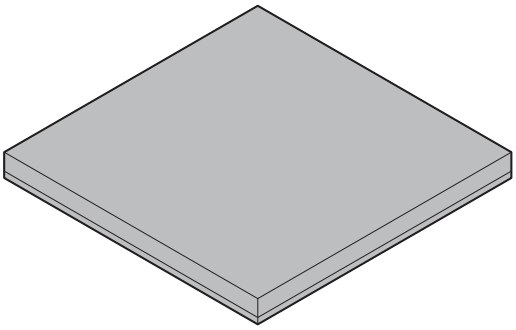
Note : Temperature : the top of the package body

(2) Manual soldering (partial heating method)

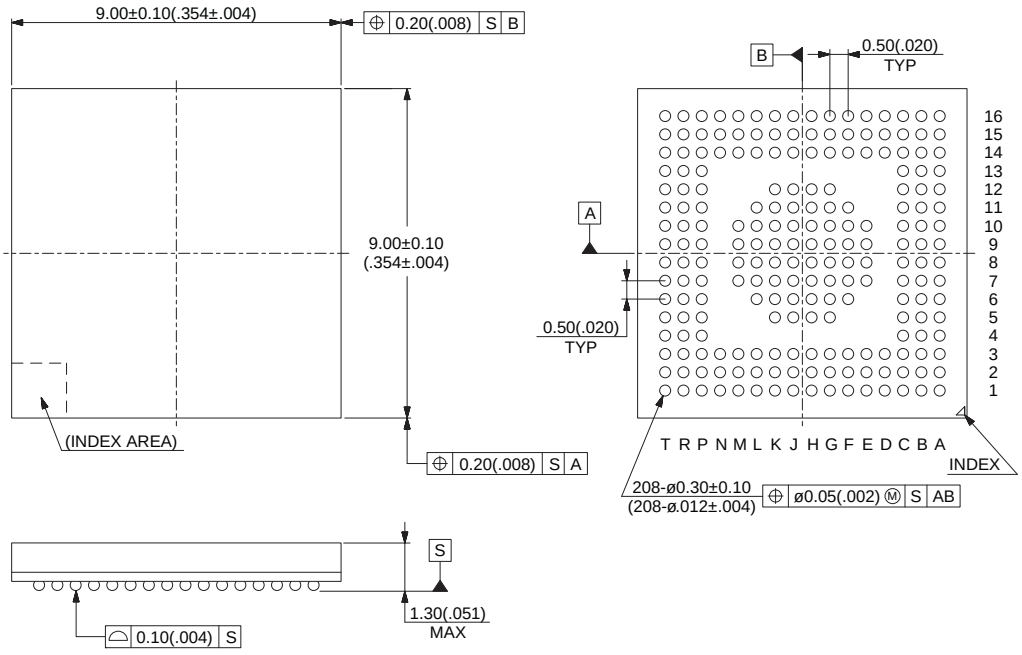
Conditions : Temperature 400 °C Max

Times : 5 s max/pin

■ PACKAGE DIMENSION

208-ball plastic PFBGA		
	Ball pitch	0.50 mm
	Package width × package length	9.00 mm × 9.00 mm
	Lead shape	Ball
	Sealing method	Plastic mold
	Mounting height	1.30 mm Max.
	Weight	0.10 g
(BGA-208P-M02)		

208-ball plastic PFBGA
(BGA-208P-M02)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest Package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

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