19-2542; Rev 0; 7/02

MAXIM

1:5 Clock Driver with Selectable LVPECL Inputs/Single-Ended Inputs and LVDS Outputs

General Description

The MAX9310A is a fast, low-skew 1:5 differential driver with selectable LVPECL inputs and LVDS outputs, designed for clock distribution applications. This device features an ultra-low propagation delay of 340ps with 48mA of supply current.

The MAX9310A operates from a 3V to 3.6V power supply for use in 3.3V systems. A 2:1 input multiplexer is used to select one of two differential inputs. The input selection is controlled through the CLKSEL pin.

This device features a synchronous enable function. The MAX9310A LVPECL inputs can be driven by either a differential or single-ended signal. A V_{BB} reference voltage output is provided for use with single-ended inputs. The device can also accept differential HSTL signals.

The MAX9310A is offered in a space-saving 20-pin TSSOP package and operates over the extended temperature range from -40°C to +85°C.

Applications

Data and Clock Drivers and Buffers

Central-Office Backplane Clock Distribution

DSLAM

Base Stations

ATE

Features

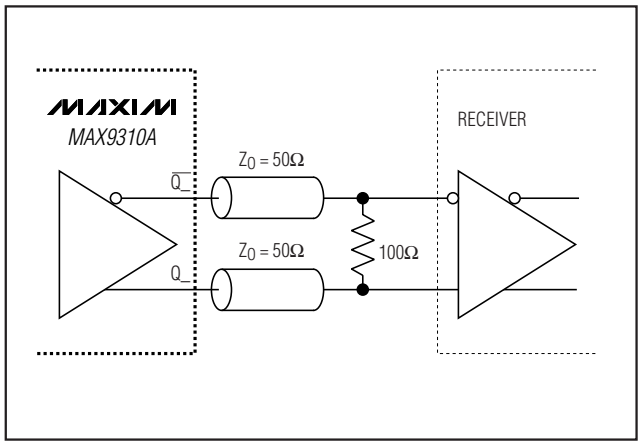
- **Guaranteed 1.0GHz Operating Frequency**
- **8.0ps Output-to-Output Skew**
- **340ps Propagation Delay**
- **Accepts LVPECL and Differential HSTL Inputs**
- **Synchronous Output Enable/Disable**
- **Two Selectable Differential Inputs**
- **3V to 3.6V Supply Voltage**
- **On-Chip Reference for Single-Ended Operation**
- **ESD Protection: ±2kV (Human Body Model)**
- **Input Bias Resistors Drive Output Low for Open Inputs**

Ordering Information

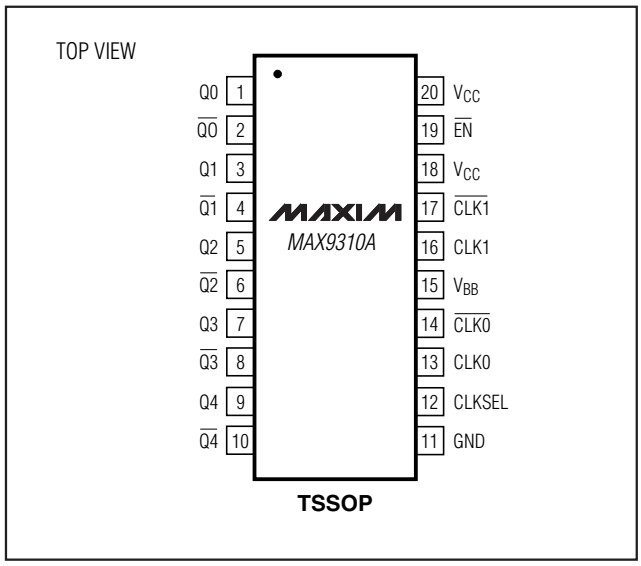
PART	TEMP RANGE	PIN-PACKAGE
MAX9310AEUP	-40°C to +85°C	20 TSSOP

Functional Diagram appears at end of data sheet.

Typical Application Circuit



Pin Configuration



1:5 Clock Driver with Selectable LVPECL Inputs/Single-Ended Inputs and LVDS Outputs

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4.1V
$\overline{EN}$, CLKSEL, CLK_, $\overline{CLK\_}$, to GND.....-0.3V to (V_{CC} + 0.3V)
CLK_ to $\overline{CLK\_}$.....±3V
Continuous Output Current.....24mA
Surge Output Current.....50mA
V_{BB} Sink/Source Current .....±0.65mA
Continuous Power Dissipation (T_A = +70°C)
Single-Layer PC Board
20-Pin TSSOP (derate 7.69mW/°C above +70°C) 615mW
Multilayer PC Board
20-Pin TSSOP (derate 11mW/°C above +70°C) 879mW
Junction-to-Ambient Thermal Resistance in Still Air
Single-Layer PC Board
20-Pin TSSOP .....+130°C/W
Multilayer PC Board
20-Pin TSSOP .....+91°C/W
Junction-to-Ambient Thermal Resistance with 500LFPM
Airflow Single-Layer PC board
20-Pin TSSOP .....+96°C/W
Junction-to-Case Thermal Resistance
20-Pin TSSOP .....+20°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection
Human Body Model (inputs and outputs) .....±2kV
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} - GND = 3V to 3.6V, outputs terminated with 100Ω ±1%, unless otherwise noted. Typical values are at V_{CC} - GND = 3.3V, V_{IHD} = V_{CC} - 1.0V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SINGLE-ENDED INPUTS (CLKSEL, $\overline{EN}$)												
Input High Voltage	V_{IH}		V_{CC} - 1.165		V_{CC} - 0.88	V_{CC} - 1.165		V_{CC} - 0.88	V_{CC} - 1.165		V_{CC} - 0.88	V
Input Low Voltage	V_{IL}		V_{CC} - 1.81		V_{CC} - 1.475	V_{CC} - 1.81		V_{CC} - 1.475	V_{CC} - 1.81		V_{CC} - 1.475	V
Input Current	I_{IN}	$V_{IH(MAX)}$, $V_{IL(MAX)}$	-10		+70	-10		+70	-10		+70	µA
DIFFERENTIAL INPUTS (CLK_, $\overline{CLK\_}$)												
Single-Ended Input High Voltage	V_{IH}	Figure 1	V_{CC} - 1.125		V_{CC} - 0.88	V_{CC} - 1.165		V_{CC} - 0.88	V_{CC} - 1.165		V_{CC} - 0.88	V
Single-Ended Input Low Voltage	V_{IL}	Figure 1	V_{CC} - 1.81		V_{CC} - 1.475	V_{CC} - 1.81		V_{CC} - 1.475	V_{CC} - 1.81		V_{CC} - 1.495	V
Differential Input High Voltage	V_{IHD}	Figure 2	1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	V
Differential Input Low Voltage	V_{ILD}	Figure 2	GND		V_{CC} - 0.095	GND		V_{CC} - 0.095	GND		V_{CC} - 0.095	V
Differential Input Voltage	V_{ID}	V_{IHD} - V_{ILD}	0.095		3.0	0.095		3.0	0.095		3.0	V
Input Current	I_{IH}, I_{IL}	CLK_, or $\overline{CLK\_}$ = V_{IHD} or V_{ILD}	-100		+100	-100		+100	-100		+100	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} - GND = 3V to 3.6V, outputs terminated with 100Ω ±1%, unless otherwise noted. Typical values are at V_{CC} - GND = 3.3V, V_{IHD} = V_{CC} - 1.0V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUTS (Q_, $\overline{Q\_}$)												
Output High Voltage	V_{OH}	Figure 2			1.6			1.6			1.6	V
Output Low Voltage	V_{OL}	Figure 2	0.9			0.9			0.9			V
Differential Output Voltage	V_{OD}	V_{OH} - V_{OL}, Figure 2	250	350	450	250	350	450	250	350	450	mV
Change in V_{OD} Between Complementary Output States	ΔV_{OD}				50			50			50	mV
Output Offset Voltage	V_{OS}		1.125	1.25	1.375	1.125	1.25	1.375	1.125	1.25	1.375	mV
Change in VOS Between Complementary Output States	ΔVOCM				25			25			25	mV
Output Short-Circuit Current	I_{OSC}	Q_ shorted to $\overline{Q\_}$			12			12			12	mA
		Q_ or $\overline{Q\_}$ shorted to GND			29			29			29	
REFERENCE												
Reference Voltage Output	V_{BB}	I_{BB} = ±0.65mA (Note 4)	V_{CC} - 1.38		V_{CC} - 1.22	V_{CC} - 1.38		V_{CC} - 1.26	V_{CC} - 1.40		V_{CC} - 1.26	V
POWER SUPPLY												
Power-Supply Current	I_{CC}	(Note 5)		45	75		48	75		51	75	mA

1:5 Clock Driver with Selectable LVPECL Inputs/Single-Ended Inputs and LVDS Outputs

AC ELECTRICAL CHARACTERISTICS

(V_{CC} - GND = 3V to 3.6V, outputs terminated with 100Ω ±1%, f_{IN} ≤ 1.0GHz, input transition time = 125ps (20% to 80%), V_{IHD} - V_{ILD} = 0.15V to V_{CC}, unless otherwise noted. Typical values are at V_{CC} - GND = 3.3V, V_{IHD} = V_{CC} - 1.0V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 1 and 6)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay CLK_, $\overline{CLK\_}$ to Q_, $\overline{Q\_}$	t_{PHL}, t_{PLH}	Figure 2	250	340	600	250	340	600	250	340	600	ps
Output-to-Output Skew	t_{SKOO}	(Note 7)		10	30		8	25		20	45	ps
Part-to-Part Skew	t_{SKPP}	(Note 8)			145			145			145	ps
Added Random Jitter	t_{RJ}	f_{IN} = 1.0GHz, clock pattern (Note 9)		0.3	1.0		0.3	1.0		0.3	1.0	ps (RMS)
Added Deterministic Jitter	t_{DJ}	f_{IN} = 1.0Gsps, 2^{23} - 1 PRBS pattern (Note 9)		50	60		50	60		50	60	ps (P-P)
Operating Frequency	f_{MAX}	V_{OD} ≥ 250mV	1.0			1.0			1.0			GHz
Differential Output Rise/Fall Time	$t_{R/tF}$	20% to 80%, Figure 2	140	205	300	140	205	300	140	205	300	ps

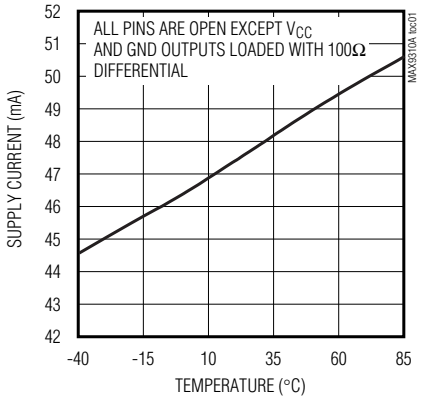
Note 1: Measurements are made with the device in thermal equilibrium.
Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.
Note 3: DC parameters are production tested at +25°C. DC limits are guaranteed by design and characterized over the full operating temperature range.
Note 4: Use V_{BB} only for inputs that are on the same device as the V_{BB} reference.
Note 5: All pins are open except V_{CC} and GND, all outputs are loaded with 100Ω differentially.
Note 6: Guaranteed by design and characterization. Limits are set to ±6 sigma.
Note 7: Measured between outputs of the same part at the signal crossing points for a same-edge transition.
Note 8: Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.
Note 9: Device jitter added to the input signal.

1:5 Clock Driver with Selectable LVPECL Inputs/Single-Ended Inputs and LVDS Outputs

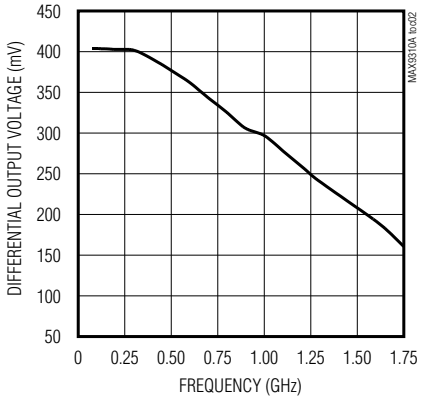
Typical Operating Characteristics

(V_{CC} - GND = 3.3V, outputs terminated with 100Ω ±1%, f_{IN} = 1.0GHz, input transition time = 125ps (20% to 80%), V_{IHD} = V_{CC} - 1.0V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.)

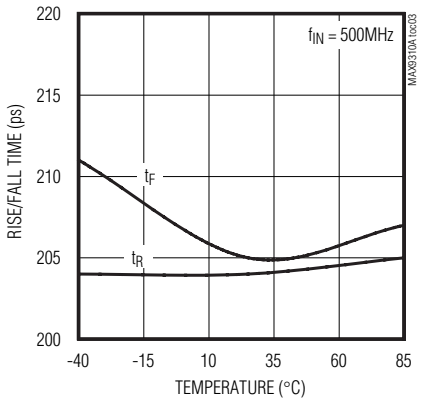
SUPPLY CURRENT vs. TEMPERATURE



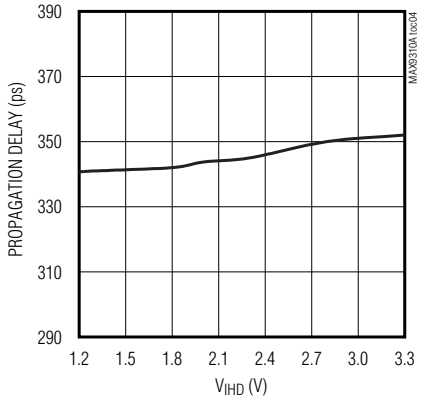
DIFFERENTIAL OUTPUT VOLTAGE (V_{OH} - V_{OL}) vs. FREQUENCY



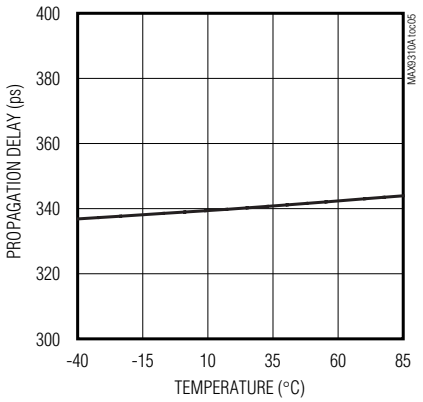
OUTPUT RISE/FALL vs. TEMPERATURE



PROPAGATION DELAY vs. HIGH VOLTAGE OF DIFFERENTIAL INPUT (V_{IHD})



PROPAGATION DELAY vs. TEMPERATURE



1:5 Clock Driver with Selectable LVPECL Inputs/Single-Ended Inputs and LVDS Outputs

Pin Description

PIN	NAME	FUNCTION
1	Q0	Noninverting Differential Output 0. Typically terminated with 100Ω to $\overline{Q0}$.
2	$\overline{Q0}$	Inverting Differential Output 0. Typically terminated with 100Ω to Q0.
3	Q1	Noninverting Differential Output 1. Typically terminated with 100Ω to $\overline{Q1}$.
4	$\overline{Q1}$	Inverting Differential Output 1. Typically terminated with 100Ω to Q1.
5	Q2	Noninverting Differential Output 2. Typically terminated with 100Ω to $\overline{Q2}$.
6	$\overline{Q2}$	Inverting Differential Output 2. Typically terminated with 100Ω to Q2.
7	Q3	Noninverting Differential Output 3. Typically terminated with 100Ω to $\overline{Q3}$.
8	$\overline{Q3}$	Inverting Differential Output 3. Typically terminated with 100Ω to Q3.
9	Q4	Noninverting Differential Output 4. Typically terminated with 100Ω to $\overline{Q4}$.
10	$\overline{Q4}$	Inverting Differential Output 4. Typically terminated with 100Ω to Q4.
11	GND	Ground
12	CLKSEL	Clock Select Input. Drive low to select the CLK0, $\overline{CLK0}$ input. Drive high to select the CLK1, $\overline{CLK1}$ input. The CLKSEL threshold is equal to V_{BB}. Internal 60kΩ pulldown to GND.
13	CLK0	Noninverting Differential Clock Input 0. Internal 75kΩ pulldown to GND.
14	$\overline{CLK0}$	Inverting Differential Clock Input 0. Internal 75kΩ pullup to V_{CC} and 75kΩ pulldown to GND.
15	V_{BB}	Reference Output Voltage. Connect to the inverting or noninverting clock input to provide a reference for single-ended operation. When used, bypass with a 0.01µF ceramic capacitor to V_{CC}; otherwise, leave open.
16	CLK1	Noninverting Differential Input 1. Internal 75kΩ pulldown to GND.
17	$\overline{CLK1}$	Inverting Differential Input 1. Internal 75kΩ pullup to V_{CC} and 75kΩ pulldown to GND.
18, 20	V_{CC}	Positive Supply Voltage. Bypass V_{CC} to GND with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
19	$\overline{EN}$	Output Enable Input. Outputs are synchronously enabled on the falling edge of the selected clock input when $\overline{EN}$ is low. Outputs are synchronously driven to a differential low state on the falling edge of the selected clock input when $\overline{EN}$ is high. Internal 60kΩ pulldown to GND (Figure 3).

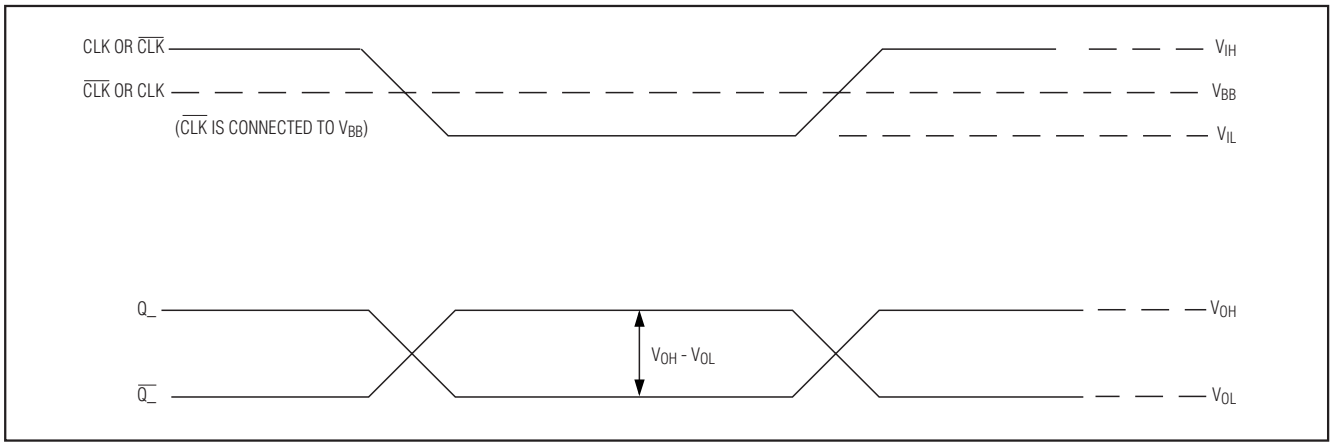


Figure 1. MAX9310A Switching Characteristics with Single-Ended Input

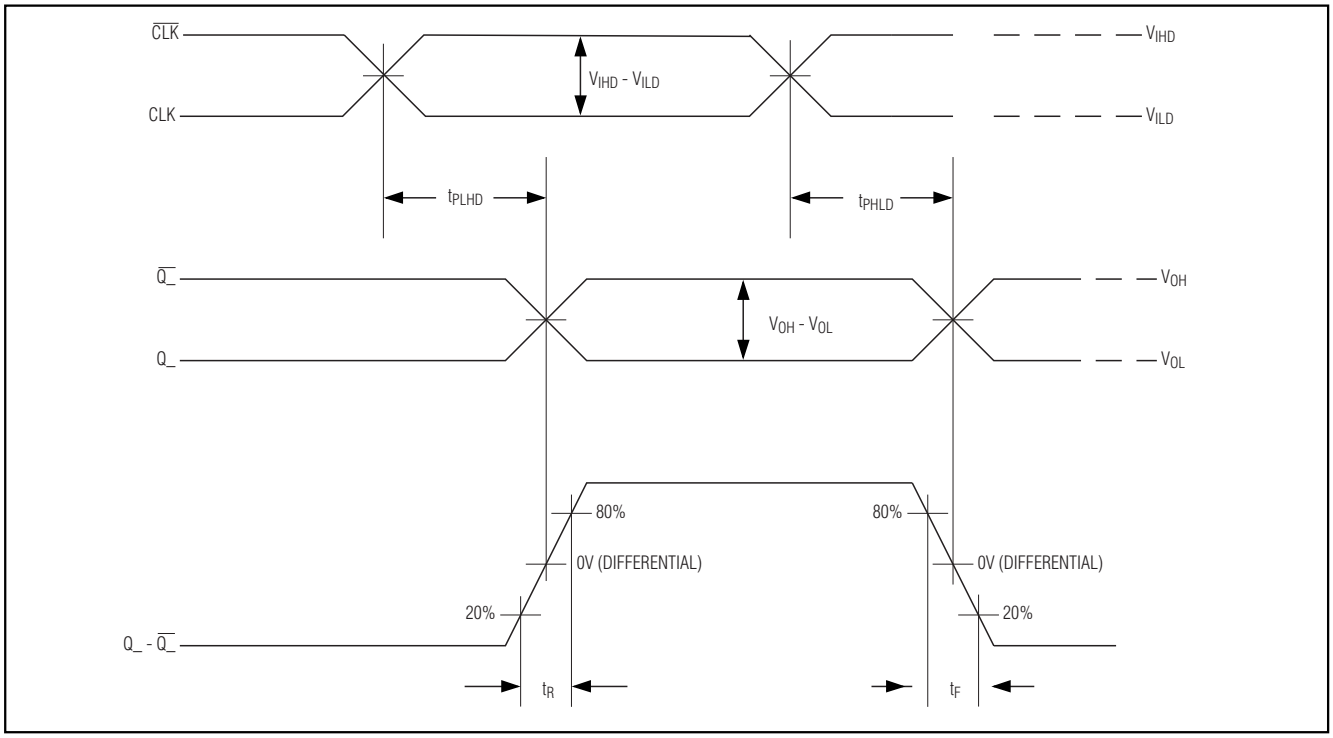


Figure 2. MAX9310A Timing Diagram

1:5 Clock Driver with Selectable LVPECL Inputs/Single-Ended Inputs and LVDS Outputs

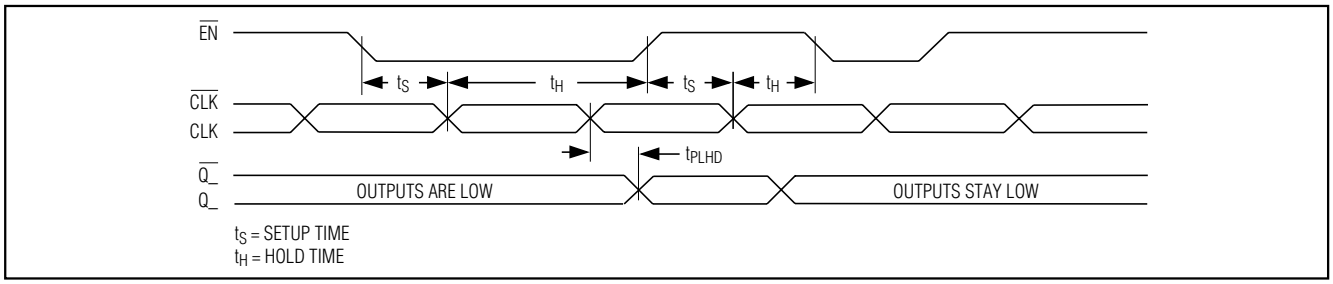


Figure 3. MAX9310A Timing $\overline{EN}$ Diagram

Detailed Description

The MAX9310A is a low-skew 1:5 differential driver with two selectable LVPECL inputs and LVDS outputs, designed for clock distribution applications. The selected clock accepts a differential input signal and reproduces it on five separate differential LVDS outputs. The inputs are biased with internal resistors such that the output is differential low when inputs are open. An on-chip V_{BB} reference output is available for single-ended input operation. The device is guaranteed to operate at frequencies up to 1.0GHz with LVDS output levels conforming to the EIA/TIA-644 standard.

The MAX9310A is designed for 3V to 3.6V operation in systems with a nominal 3.3V supply.

Differential LVPECL Input

The MAX9310A has two input differential pairs that accept differential LVPECL/HSTL inputs, and can be configured to accept single-ended LVPECL inputs through the use of the V_{BB} voltage-reference output. Each differential input pair has to be independently terminated. A select pin (CLKSEL) is used to activate the desired input. The maximum magnitude of the differential signal applied to the input is 3V. Specifications for the high and low voltages of a differential input (V_{IHD} and V_{ILD}) and the differential input voltage (V_{IHD} - V_{ILD}) apply simultaneously.

Single-Ended Inputs and V_{BB}

The differential inputs can be configured to accept a single-ended input through the use of the V_{BB} reference voltage. A noninverting, single-ended input is produced by connecting V_{BB} to the $\overline{CLK\_}$ input and applying a single-ended signal to the CLK_ input. Similarly, an inverting input is produced by connecting V_{BB} to the CLK_ input and applying the signal to the $\overline{CLK\_}$ input. With a differential input configured as single ended (using V_{BB}), the single-ended input can be driven to V_{CC} and GND, or with a single-ended LVPECL signal. Note the single-ended input must be at least V_{BB} ±95mV or a differential input of at least 95mV to switch the outputs to the V_{OH} and V_{OL} levels specified in the *DC Electrical Characteristics* table (Figure 1).

When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC}. If the V_{BB} reference is not used, leave unconnected. The V_{BB} reference can source or sink 500µA. Use V_{BB} only for inputs that are on the same device as the V_{BB} reference.

Synchronous Enable

The MAX9310A is synchronously enabled and disabled with outputs in a differential low state to eliminate shortened clock pulses. $\overline{EN}$ is connected to the input of an edge-triggered D flip-flop. After power-up, drive $\overline{EN}$ low and toggle the selected clock input to enable the outputs. The outputs are enabled on the falling edge of the selected clock input after $\overline{EN}$ goes low. The outputs are set to a differential low state on the falling edge of the selected clock input after $\overline{EN}$ goes high (Figure 3).

Input Bias Resistors

Internal biasing resistors ensure a (differential) output low condition in the event that the inputs are not connected. The inverting input ($\overline{CLK\_}$) is biased with a 75kΩ pulldown to GND and a 75kΩ pullup to V_{CC}. The noninverting input (CLK_) is biased with a 75kΩ pulldown to GND.

Differential LVDS Output

The LVDS outputs must be terminated with 100Ω across Q and $\overline{Q}$, as shown in the *Typical Application Circuit*. The outputs are short-circuit protected.

Applications Information

Supply Bypassing

Bypass each V_{CC} to GND with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors in parallel as close to the device as possible, with the 0.01µF capacitor closest to the device. Use multiple parallel vias to minimize parasitic inductance. When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC}. If the V_{BB} reference is not used, it can be left open.

Controlled-Impedance Traces

Input and output trace characteristics affect the performance of the MAX9310A. Connect high-frequency input and output signals to 50Ω characteristic impedance traces. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through cables and connectors. Reduce skew within a differential pair by matching the electrical length of the traces.

Output Termination

Terminate the outputs with 100Ω across Q_ and $\overline{Q}$_, as shown in the *Typical Application Circuit*.

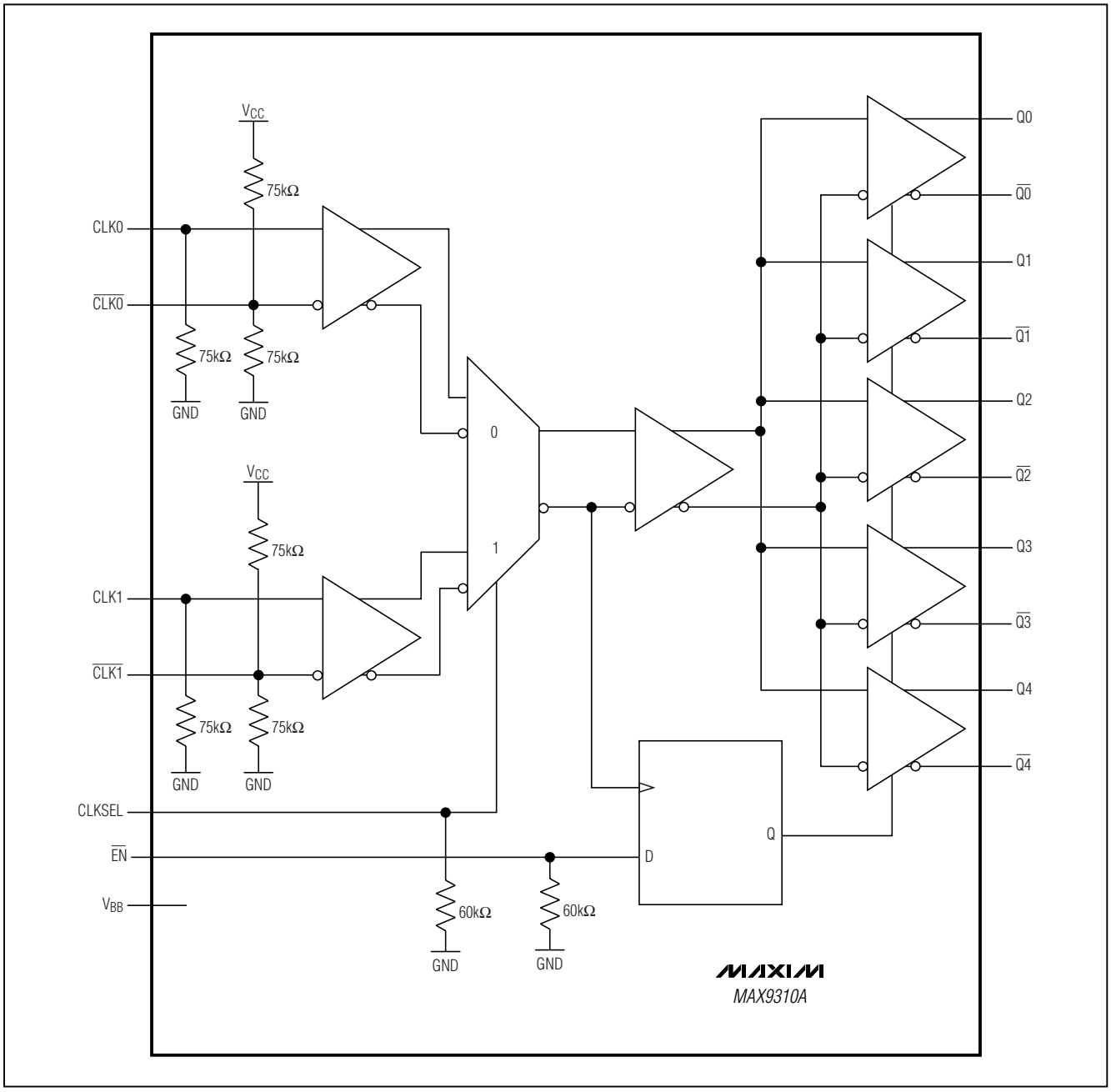
Chip Information

TRANSISTOR COUNT: 716

PROCESS: Bipolar

1:5 Clock Driver with Selectable LVPECL Inputs/Single-Ended Inputs and LVDS Outputs

Functional Diagram

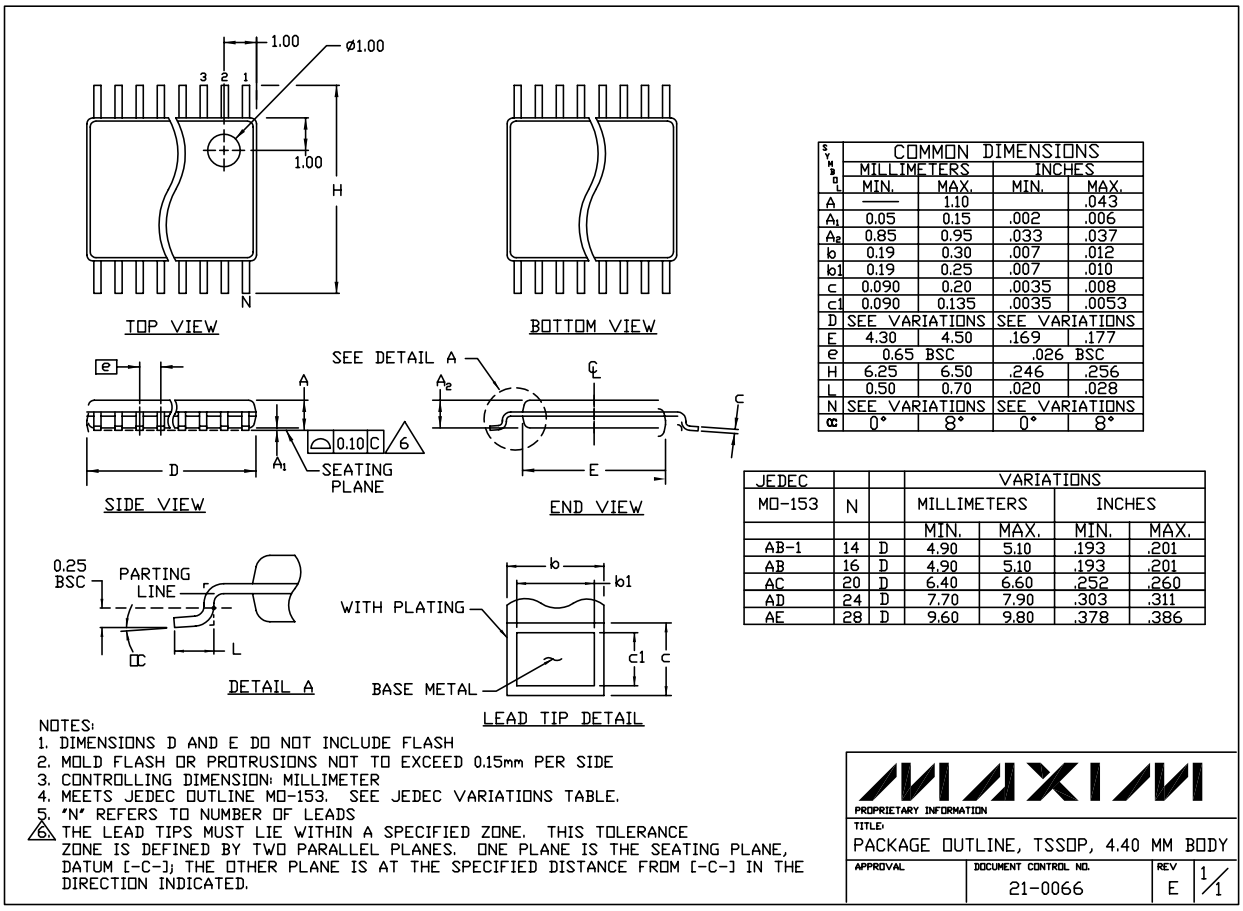


1:5 Clock Driver with Selectable LVPECL Inputs/Single-Ended Inputs and LVDS Outputs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP,NO PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0066	E	1/1