ROHM
SEMICONDUCTOR

STRUCTURE Silicon Monolithic Integrated Circuit

TYPE Positive and Negative Variable Linear Regulator

PRODUCT SERIES ＢＤ３９１６ＦＶＭ

FEATURES
1. Built-in positive (REG1) and negative (REG2) Linear Regulator for CCDs/ Variable output/ Low dropout voltage type.
2. Built-in Discharge circuit. Negative output voltage (REG2) turns off immediately, after STB turns off.

○ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Parameter	Symbol	Limit	Unit
Positive Supply Voltage	VCC	+18 ※1	V
Negative Supply Voltage	VEE	-18 ※1	V
Power Dissipation	Pd	470 ※2	mW
Operating Temperature Range	Topr	-40～+85	℃
Storage Temperature Range	Tstg	-55～+125	℃
Maximum Junction Temperature	Tjmax	125	℃

※1 Not to exceed Pd.
※2 Reduced by 4.7mW/℃ over Ta=25℃ ,when mount on a glass epoxy board:70mm×70mm×1.6mm。

○OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Positive Supply Voltage	VCC	+6.0	+18.0	V
Negative Supply Voltage	VEE	-14.0	-6.0	V
REG1 Output Voltage	Vo1	Vctl1 *1	+16.0	V
REG2 Output Voltage	Vo2	-8.5	Vctl2 *2	V
Output Current 1	Io1	—	25	mA
Output Current 2	Io2	—	50	mA

*1 REG1,CTL1 Short
*2 REG2,CTL2 Short
※ Vdropout(REG1) × Io(REG1) + Vdropout(REG2) × Io(REG2) not to exceed Pd=470mW.

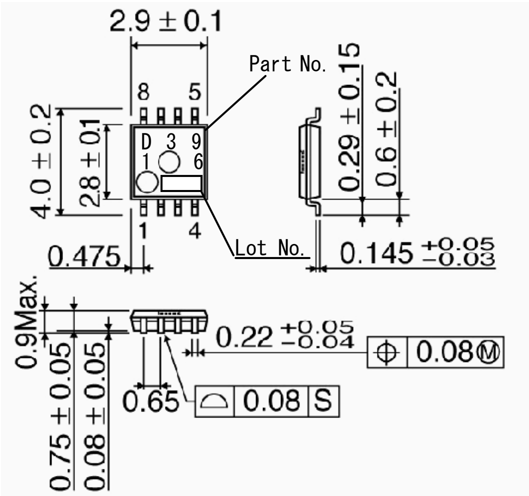
NOTE) The product described in this specification is a strategic product (and/or service) subject to COCOM regulations. It should not be exported without authorization from the appropriate government.

○ELECTRICAL CHARACTERISTICS(Unless otherwise specified, Ta=25℃, VCC=16.5V, VEE=-10V, Set REG1=15V, Set REG2=-7.5V)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	Typ	MAX		
【Bias current】						
Bias Current (VCC)	ICC	—	500	850	μA	Io1=0mA
Bias Current (VEE)	IEE	—	200	300	μA	Io2=0mA
【STB】						
STB OFF Voltage	STBOFF	0	—	0.6	V	Io1,2=0mA
STB ON Voltage	STBON	1.6	—	3.5	V	Io1,2=0mA
STB OFF Bias Current (VEE)	IOFF	0.7	1.6	2.5	mA	Io1,2=0mA
STB ON Input Current	Iin	10	30	60	μA	VSTB=2V, Io1,2=0mA
【Discharge block】						
Discharge Current	Idis	1.5	3.5	6.0	mA	
【REG1】						
CTL1 Voltage	Vctl1	1.379	1.400	1.421	V	Io1=10mA
Dropout Voltage 1	ΔVd1	—	0.25	0.35	V	Vcc=14.2V, Io1=25mA
Peak Output Current 1	Io1	25	—	—	mA	
Load Regulation 1	Vload1	—	100	—	mV	Io1=0～25mA
Short - Circuit Output Current 1	Ishort1	—	50	—	mA	Vo1=0V
Ripple Rejection 1	R.R.1	—	50	—	dB	f=120Hz, ein=1Vrms, Io1=2mA
Temperature Coefficient of Output Voltage 1	Tcvo1	—	±0.02	—	%/℃	Io1=1mA, Tj=0～125℃
【REG2】						
CTL2 Voltage	Vctl1	-1.269	-1.250	-1.231	V	Io2=10mA
Dropout Voltage2	ΔVd2	—	0.35	0.45	V	VEE=-7.1V, Io2=50mA
Peak Output Current2	Io2	50	—	—	mA	
Load Regulation2	Vload2	—	100	—	mV	Io2=0～50mA
Short - Circuit Output Current 2	Ishort2	—	120	—	mA	Vo2=0V
Ripple Rejection2	R.R.2	—	50	—	dB	f=120Hz, ein=1Vrms, Io2=2mA
Temperature Coefficient of Output Voltage 2	Tcvo2	—	±0.02	—	%/℃	Io2=1mA, Tj=0～125℃

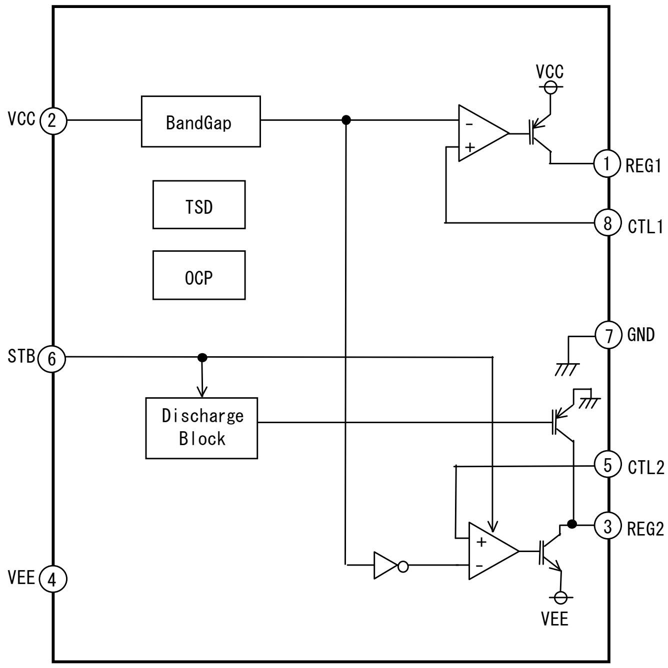
◎ Discharge time
t=(Reg2×Co)/Idis [s]   (VEE=-10V)   Co:Reg2 Output capacitor(μF)
This product is not designed for protection against radio active rays.

○PHYSICAL DIMENSIONS・MARKING



MSOP-8 (UNIT : mm)

○BLOCK DIAGRAM



※Refer to the Technical Note about the details of the application.

○PIN No.・PIN NAME

Pin No.	Pin Name
1	REG1
2	VCC
3	REG2
4	VEE
5	CTL2
6	STB
7	GND
8	CTL1

○OPERATING NOTES

1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) VEE potential
Ensure a minimum VEE pin potential in all operating conditions.

3) Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

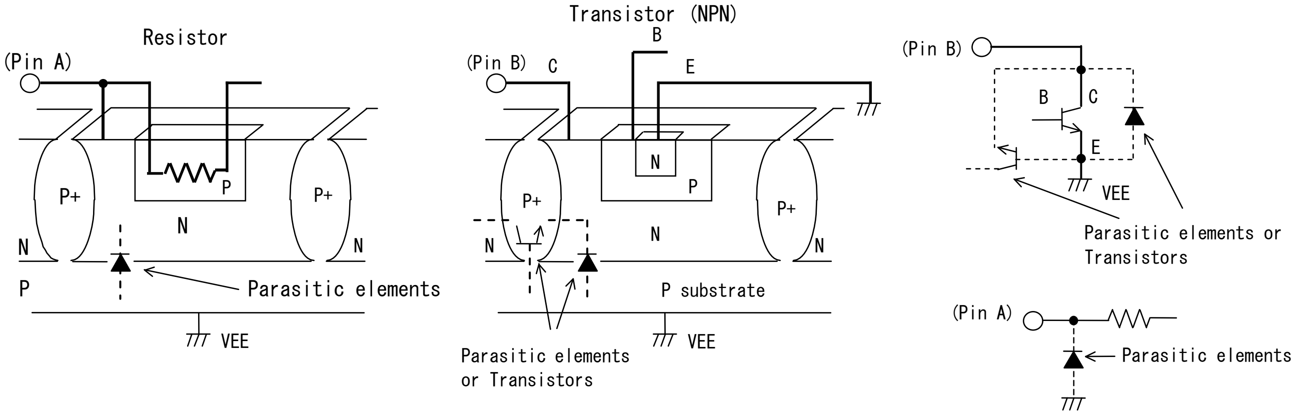
4) Pin short and mistake mounting
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC. Ensure a minimum GND pin potential in all operating conditions.

5) Actions in strong magnetic field
Keep in mind that the IC may malfunction in strong magnetic fields.

6) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

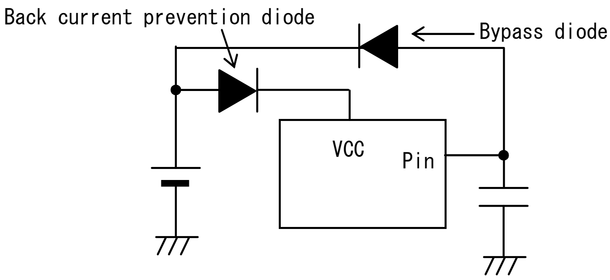
7) This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when the resistors and transistors are connected to the pins as shown in the following figure,
○The P/N junction functions as a parasitic diode when VEE > Pin A for the resistor or VEE > Pin B for the transistor (NPN).
○Similarly, when VEE > Pin B for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the VEE (P substrate) voltage to input pins. Keep in mind that the IC may malfunction in strong magnetic fields.



8) Ground patterns
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external parts, either.

9) Applications or inspection processes where the potentials of the VCC pin and other pins may be reversed from their normal states may cause damage to the IC's internal circuitry or elements. Use an output pin capacitance of 1,000μF or lower in case VCC is shorted with the GND pin while the external capacitor is charged. It is recommended to insert a diode for preventing back current flow in series with VCC or bypass diodes between VCC and each pin.



10) Thermal shutdown circuit (TSD)
This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the junction temperature (Tj) will trigger the TSD circuit to turn off all output power elements.
The circuit automatically resets once the junction temperature (Tj) drops. Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

11) Overcurrent protection circuit (OCP)
The IC incorporates a built-in overcurrent protection circuit that operates according to the output current capacity. This circuit serves to protect the IC from damage when the load is shorted. The protection circuit is designed to limit current flow by not latching in the event of a large and instantaneous current flow originating from a large capacitor or other component. This protection circuits is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

Notes

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